

## Common-Drain Dual N-Channel MOSFET

### DESCRIPTION

SMC8205AGW is the Dual N-Channel MOSFET, this advanced trench technology to provide excellent  $R_{DS(ON)}$ , facilitated by its common-drain as a Unidirectional or bidirectional load switch applications.

### PART NUMBER INFORMATION

**SMC 8205AG W - TR G**  
 a      b      c      d      e

- a : Company name.
- b : Product Serial number.
- c : Package code            W:TSSOP-8
- d : Handling code            TR:Tape&Reel
- e : Green produce code    G:RoHS Compliant

### FEATURES

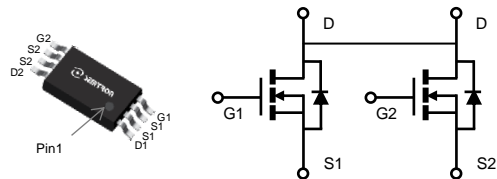
**$V_{DS}=20V, I_D=6.4A$**

- $R_{DS(ON)}=21m\Omega(Typ.)@V_{GS}=4.5V$
- $R_{DS(ON)}=22m\Omega(Typ.)@V_{GS}=4.0V$
- $R_{DS(ON)}=23m\Omega(Typ.)@V_{GS}=3.2V$
- $R_{DS(ON)}=25m\Omega(Typ.)@V_{GS}=2.5V$

- ◆ Fast switch
- ◆ High power and current handling capability
- ◆ Exceptional on-resistance

### APPLICATIONS

- ◆ Unidirectional / bidirectional Portable Equipment and Battery Powered.



TSSOP-8

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter	Rating	Units	
$V_{DSS}$	Drain-Source Voltage	20	V	
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	V	
$I_D$	Continuous Drain Current ( $V_{GS}=4.5V$ )	$T_A=25^\circ C$	6.4	A
		$T_A=70^\circ C$	5.1	A
$I_{DM}$	Pulsed Drain Current <sup>B</sup>	25.6	A	
$P_D$	Power Dissipation <sup>A</sup>	$T_A=25^\circ C$	1.6	W
		$T_A=70^\circ C$	1	W
$T_J$	Operation Junction Temperature	-55/150	$^\circ C$	
$T_{STG}$	Storage Temperature Range	-55/150	$^\circ C$	

### THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>A</sup>	$t \leq 10s$	80	$^\circ C/W$
	Thermal Resistance Junction to Ambient <sup>AC</sup>	Steady-State	120	

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ Unless otherwise noted)

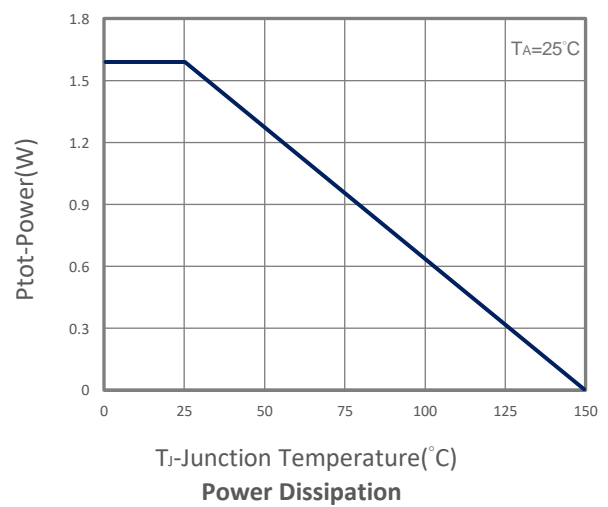
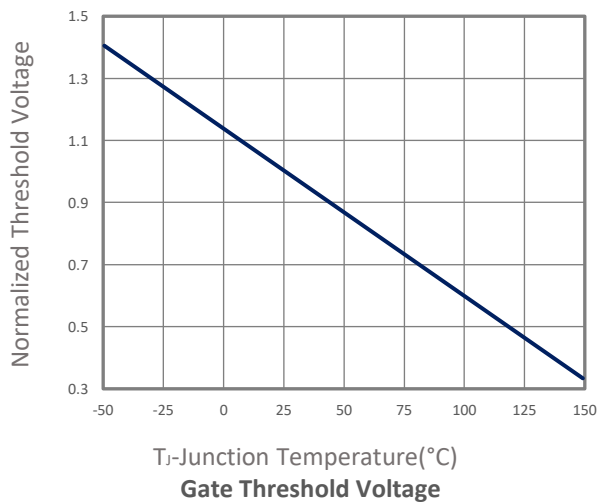
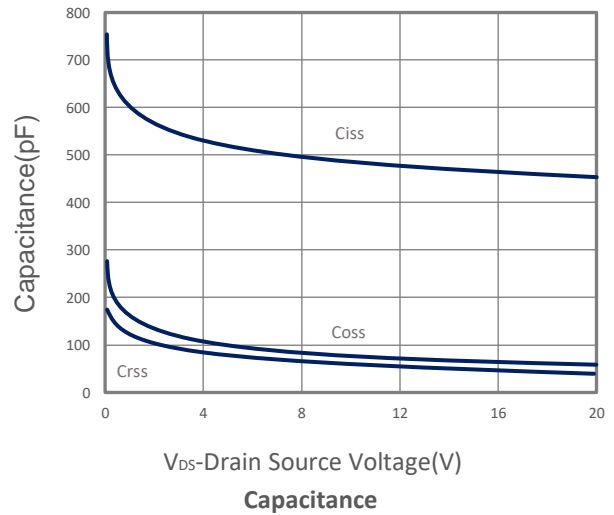
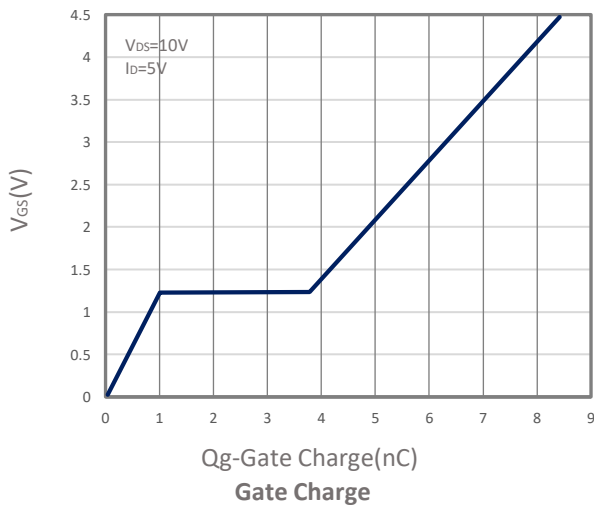
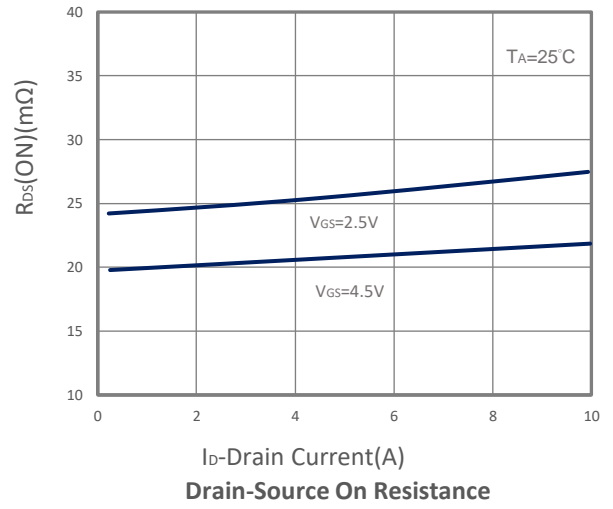
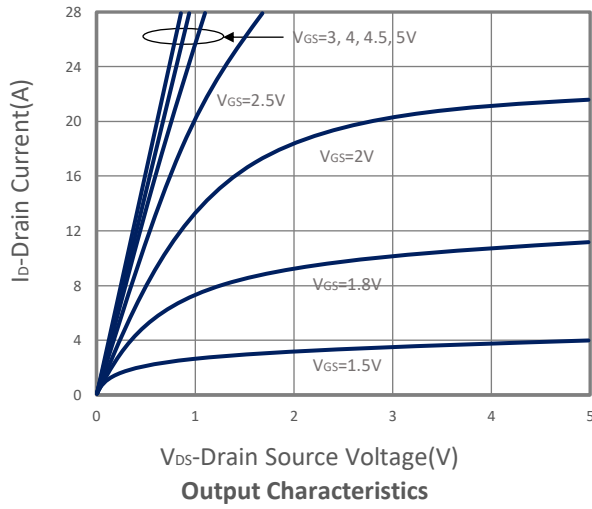
Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Static Parameters</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 $\mu$ A	20			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 $\mu$ A	0.4	0.7	1.0	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = $\pm$ 12V,			$\pm$ 100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, T <sub>J</sub> =25 $^\circ$ C			1	$\mu$ A
		V <sub>DS</sub> =16V, V <sub>GS</sub> =0V, T <sub>J</sub> =75 $^\circ$ C			10	
R <sub>DS(ON)</sub>	Drain-source On-Resistance <sup>D</sup>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =6.4A		21	25	m $\Omega$
		V <sub>GS</sub> =4.0V, I <sub>D</sub> =5A		22	26	
		V <sub>GS</sub> =3.2V, I <sub>D</sub> =4A		23	28	
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =3A		25	30	
G <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =5A		7		S
<b>Diode Characteristics</b>						
V <sub>SD</sub>	Diode Forward Voltage <sup>D</sup>	I <sub>S</sub> =1A, V <sub>GS</sub> =0V			1	V
I <sub>S</sub>	Diode Continuous Forward Current				6.4	A
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =5A, dI/dt=100A/ $\mu$ s		8.5		ns
Q <sub>rr</sub>	Reverse Recovery Charge			2.7		nC
<b>Dynamic and Switching Parameters<sup>E</sup></b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =10V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A		8.4	11.8	nC
Q <sub>gs</sub>	Gate-Source Charge			1	1.4	
Q <sub>gd</sub>	Gate-Drain Charge			2.8	3.9	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, f=1MHz		492		pF
C <sub>oss</sub>	Output Capacitance			82		
C <sub>rss</sub>	Reverse Transfer Capacitance			70		
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, F=1MHz		1.6		$\Omega$
t <sub>d(on)</sub>	Turn-On Time	V <sub>DD</sub> =10V, V <sub>GEN</sub> =4.5V R <sub>G</sub> =3.3 $\Omega$ , I <sub>D</sub> =1A		4.7	9	nS
t <sub>r</sub>				14	27	
t <sub>d(off)</sub>	Turn-Off Time			23.6	45	
t <sub>f</sub>				8.5	16	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

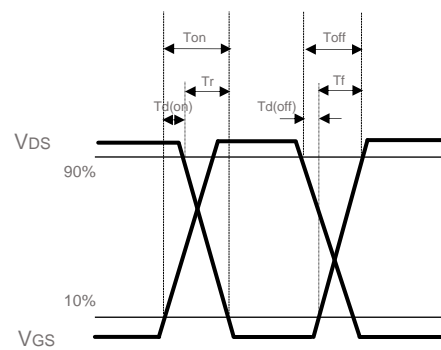
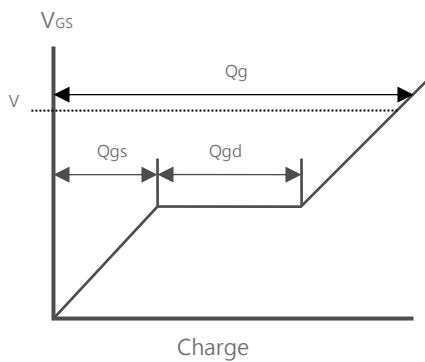
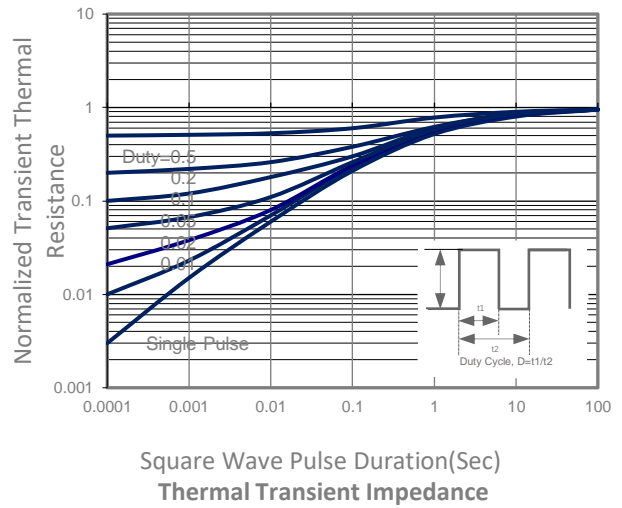
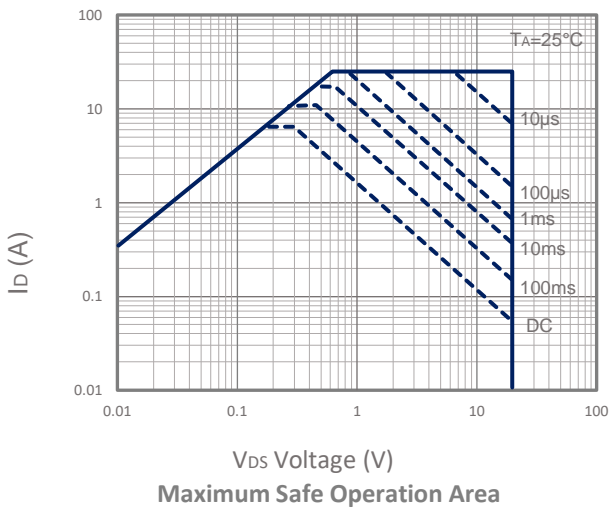
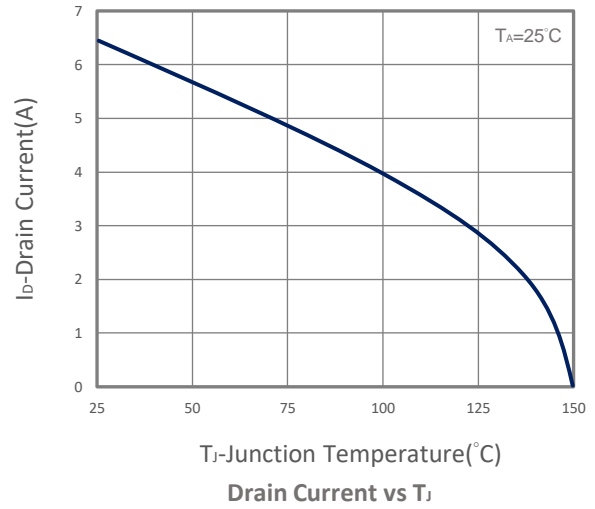
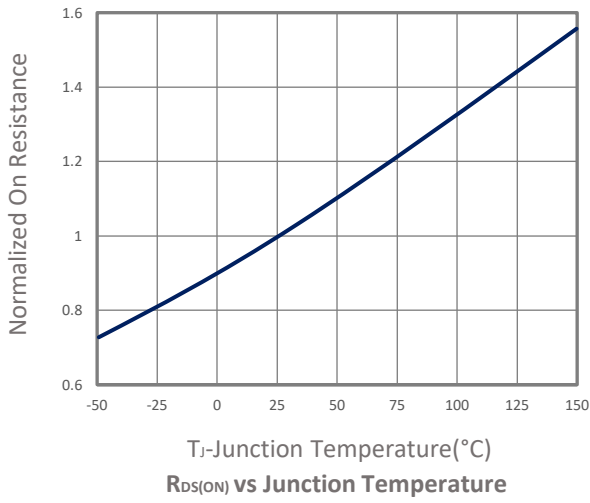
- A. Surface mounted on FR4 board using 1 in<sup>2</sup> pad size.
- B. Pulsed width limited by maximum junction temperature, T<sub>J(MAX)</sub>=150 $^\circ$ C.
- C. Using  $\leq$  10s junction-to-ambient thermal resistance is base on T<sub>J(MAX)</sub>=150 $^\circ$ C.
- D. Pulse test width  $\leq$ 300 $\mu$ s and duty cycle  $\leq$  2%.
- E. Guaranteed by design, not subject to production testing.

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## TYPICAL CHARACTERISTICS



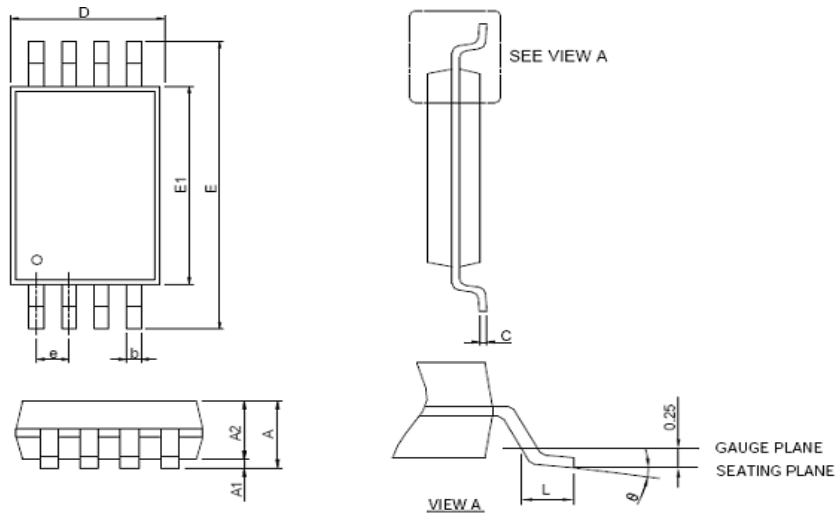
## TYPICAL CHARACTERISTICS



**Gate Charge Waveform**

**Switching Time Waveform**

## TSSOP-8 PACKAGE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	2.900	3.100	0.114	0.122
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 REF		0.026 REF	
L	0.450	0.750	0.018	0.030
theta	0°	8°	0°	8°