

Single P-Channel MOSFET

■ DESCRIPTION

SMC5225H is the P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior fast switching performance and withstand high energy pulse in the avalanche and commutation mode.

■ PART NUMBER INFORMATION

SMC 5225 H - TR G

a : Company name.
b : Product Serial number.
c : Package code H:TO-252
d : Handling code TR:Tape&Reel
e : Green produce code G:RoHS Compliant

■ FEATURES

$V_{DS}=-30V, I_D=-22A$

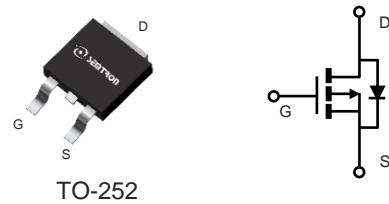
$R_{DS(ON)}=38m\Omega(Typ.)@V_{GS}=-10V$

$R_{DS(ON)}=50m\Omega(Typ.)@V_{GS}=-4.5V$

◆ High power and current handling capability

■ APPLICATIONS

- ◆ LED Application
- ◆ Power Management
- ◆ Load Switch



TO-252

■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ C$ Unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_c=25^\circ C$	-22
		$T_c=100^\circ C$	-14
I_{DM}	Pulsed Drain Current ^B	-36.8	A
I_D	Continuous Drain Current	$T_A=25^\circ C$	-9.2
		$T_A=70^\circ C$	-7.3
P_D	Power Dissipation ^A	$T_A=25^\circ C$	6.3
		$T_A=70^\circ C$	4
I_{AS}	Avalanche Current ^B	-20	A
E_{AS}	Single Pulse Avalanche energy $L=0.3mH$ ^B	60	mJ
P_D	Power Dissipation ^C	$T_c=25^\circ C$	35
		$T_c=100^\circ C$	14
T_J	Operation Junction Temperature	-55/150	°C
T_{STG}	Storage Temperature Range	-55/150	°C

■ THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^A	$t \leq 10s$	20	°C/W
	Thermal Resistance Junction to Ambient ^{AC}		50	
$R_{\theta JC}$	Thermal Resistance Junction to Case	Steady-State	3.5	

ELECTRICAL CHARACTERISTICS($T_A=25^\circ\text{C}$ Unless otherwise noted)

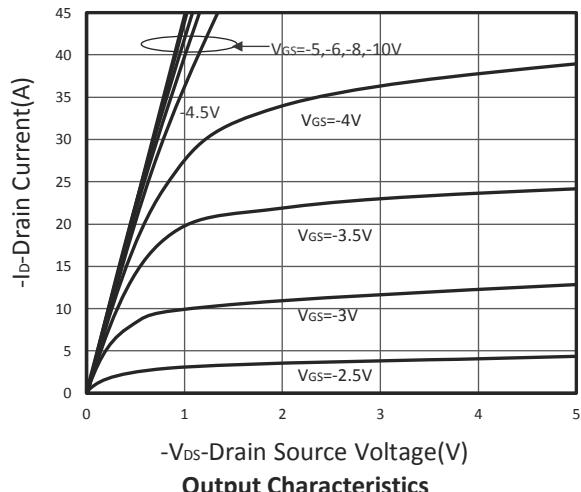
Symbol	Parameter	Condition	Min	Typ	Max	Unit	
Static Parameters							
BV_{DSS}	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=-250\mu\text{A}$	-30			V	
$\text{V}_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=-250\mu\text{A}$	-1	-1.5	-2	V	
I_{GSS}	Gate Leakage Current	$\text{V}_{\text{DS}}=0\text{V}, \text{V}_{\text{GS}}=\pm 20\text{V}$			± 100	nA	
I_{DSS}	Zero Gate Voltage Drain Current	$\text{V}_{\text{DS}}=-30\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{T}_J=25^\circ\text{C}$			-1	μA	
		$\text{V}_{\text{DS}}=-24\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{T}_J=75^\circ\text{C}$			-10		
$\text{R}_{\text{DS}(\text{ON})}$	Drain-source On-Resistance ^D	$\text{V}_{\text{GS}}=-10\text{V}, \text{I}_D=-9.2\text{A}$		38	45	$\text{m}\Omega$	
		$\text{V}_{\text{GS}}=-4.5\text{V}, \text{I}_D=-7\text{A}$		50	65		
G_{fs}	Forward Transconductance	$\text{V}_{\text{DS}}=-10\text{V}, \text{I}_D=-4.5\text{A}$		12		S	
Diode Characteristics							
V_{SD}	Diode Forward Voltage ^D	$\text{I}_S=-1\text{A}, \text{V}_{\text{GS}}=0\text{V}$			-1	V	
I_S	Diode Continuous Forward Current				-9.2	A	
t_{rr}	Revese Recovery Time	$\text{I}_S=-4.5\text{A}, \frac{d\text{I}}{dt}=100\text{A}/\mu\text{s}$		15		ns	
Q_{rr}	Reverse Recovery Charge			9.8		nC	
Dynamic and Switching Parameters ^E							
Q_g	Total Gate Charge	$\text{V}_{\text{DS}}=-15\text{V}, \text{V}_{\text{GS}}=-10\text{V}$ $\text{I}_D=-4.5\text{A}$		10	14	nC	
Q_g	Total Gate Charge (4.5V)			4.8	6.7		
Q_{gs}	Gate-Source Charge			1.8	2.5		
Q_{gd}	Gate-Drain Charge			2	2.8		
C_{iss}	Input Capacitance	$\text{V}_{\text{DS}}=-15\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{f}=1\text{MHz}$		583		pF	
C_{oss}	Output Capacitance			70			
C_{rss}	Reverse Transfer Capacitance			58			
$\text{t}_{\text{d}(\text{on})}$	Turn-On Time	$\text{V}_{\text{DD}}=-15\text{V}, \text{V}_{\text{GEN}}=-10\text{V}$ $\text{R}_G=6\Omega, \text{I}_D=-1\text{A}$		8.3		nS	
t_r				10			
$\text{t}_{\text{d}(\text{off})}$	Turn-Off Time			16.8			
t_f				7.8			

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

- A. Surface mounted on FR4 board using 1 in² pad size.
- B. Pulsed width limited by maximum junction temperature, $\text{T}_J(\text{MAX})=150^\circ\text{C}$ (initial temperature $\text{T}_J=25^\circ\text{C}$).
- C. Using $\leq 10\text{s}$ junction-to-ambient thermal resistance is base on $\text{T}_J(\text{MAX})=150^\circ\text{C}$.
- D. Pulse test width $\leq 300\mu\text{s}$ and duty cycle $\leq 2\%$.
- E. Guaranteed by design, not subject to production testing.

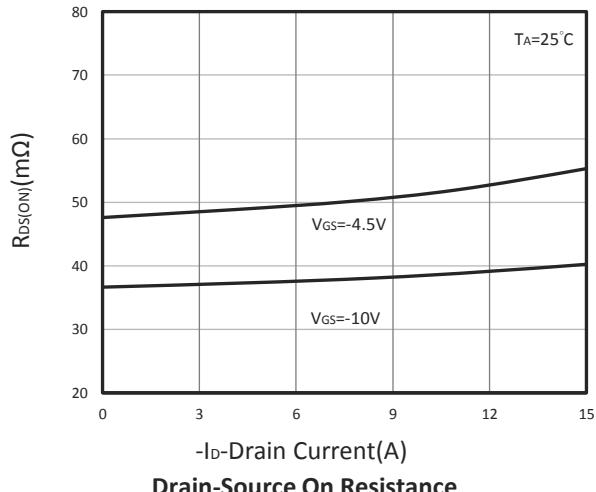
The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date. We assume no responsibility for any infringement of patents, patent rights, or other rights arising from the use of any information and circuitry in this datasheet.

■ TYPICAL CHARACTERISTICS



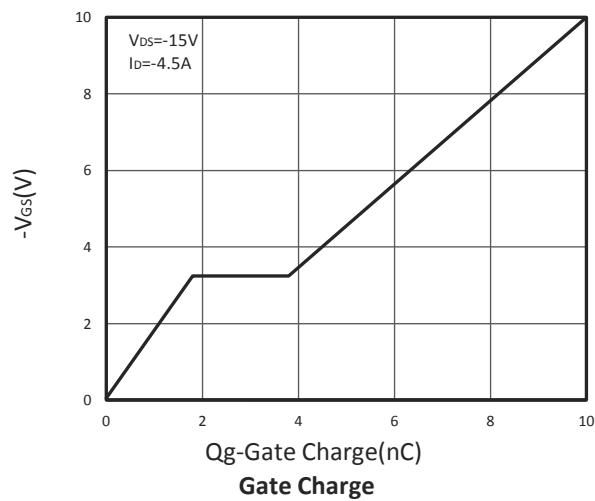
- V_{DS} -Drain Source Voltage(V)

Output Characteristics



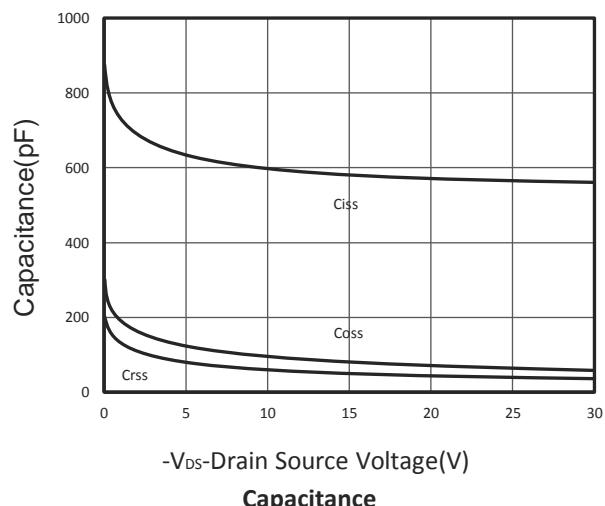
- I_D -Drain Current(A)

Drain-Source On Resistance



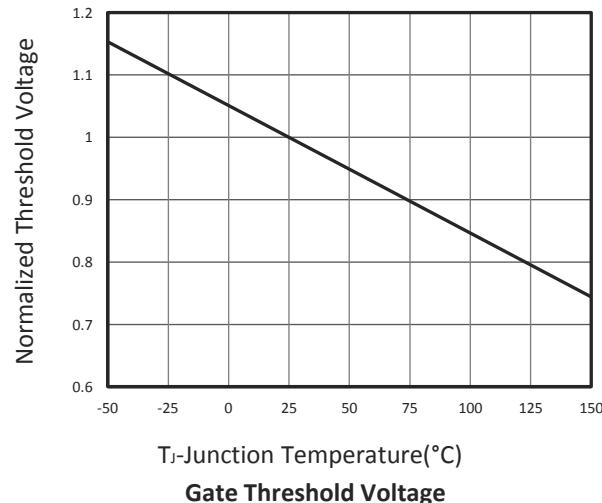
$V_{DS} = -15V$

Gate Charge



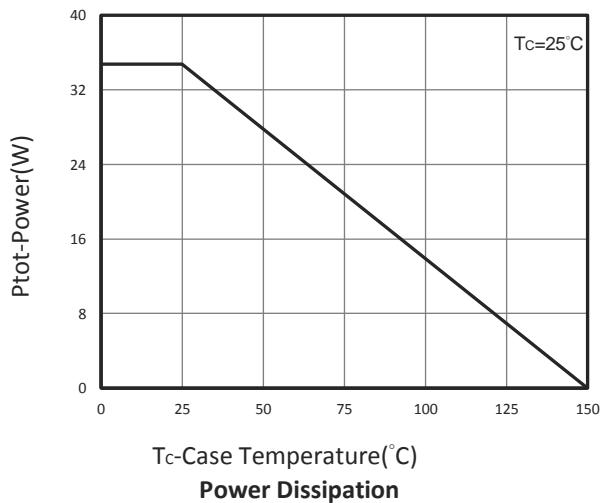
- V_{DS} -Drain Source Voltage(V)

Capacitance



T_J -Junction Temperature(°C)

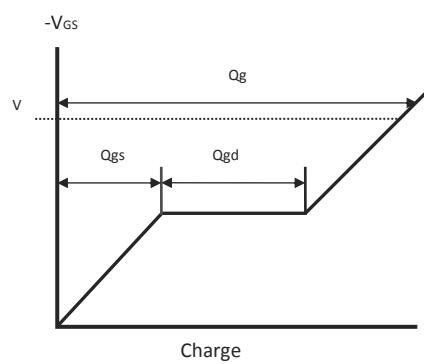
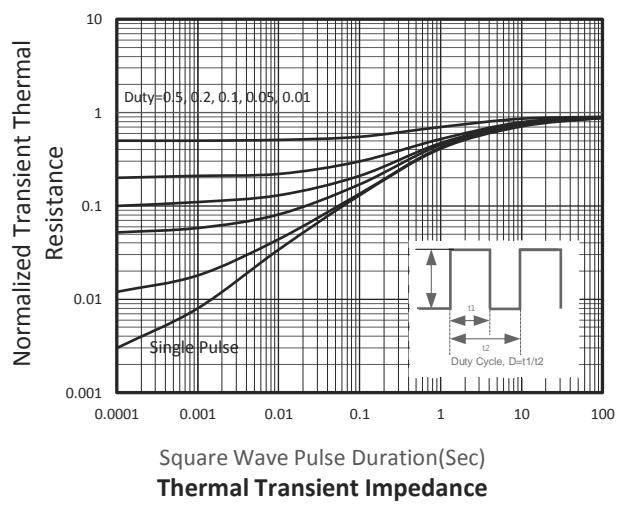
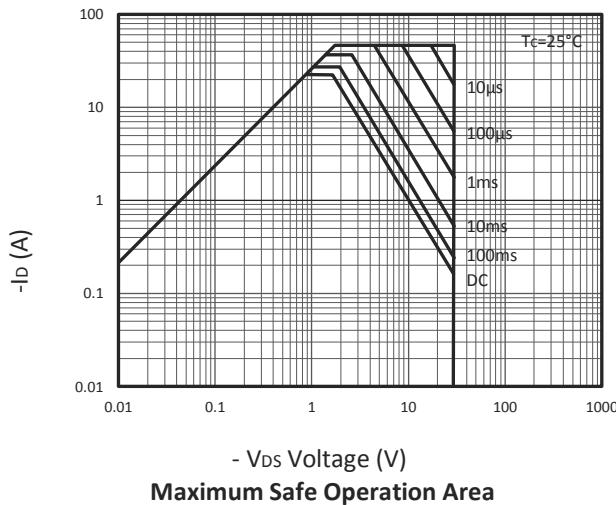
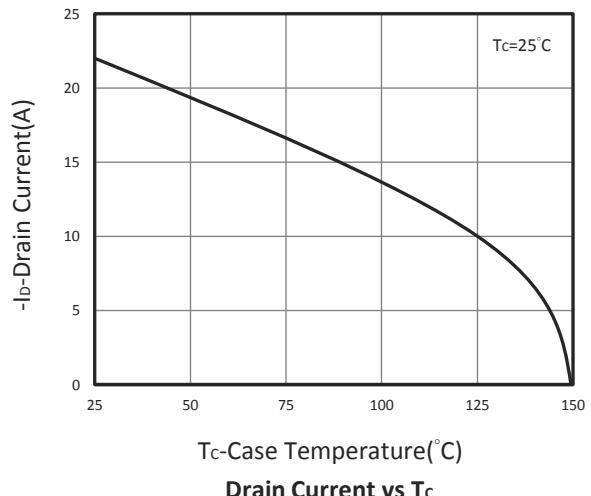
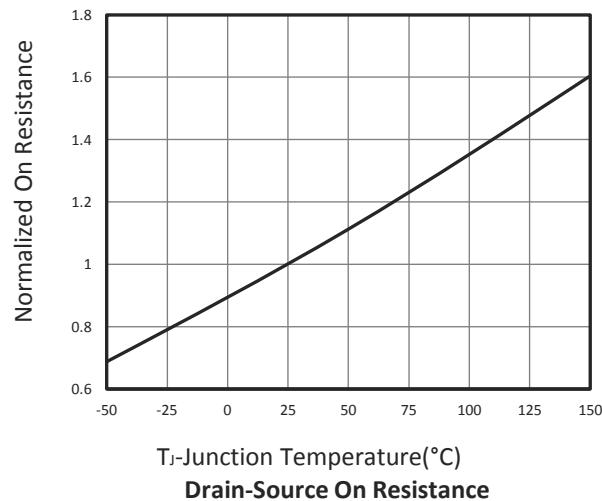
Gate Threshold Voltage



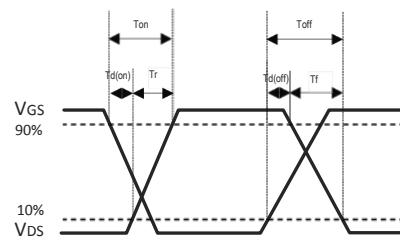
T_C -Case Temperature(°C)

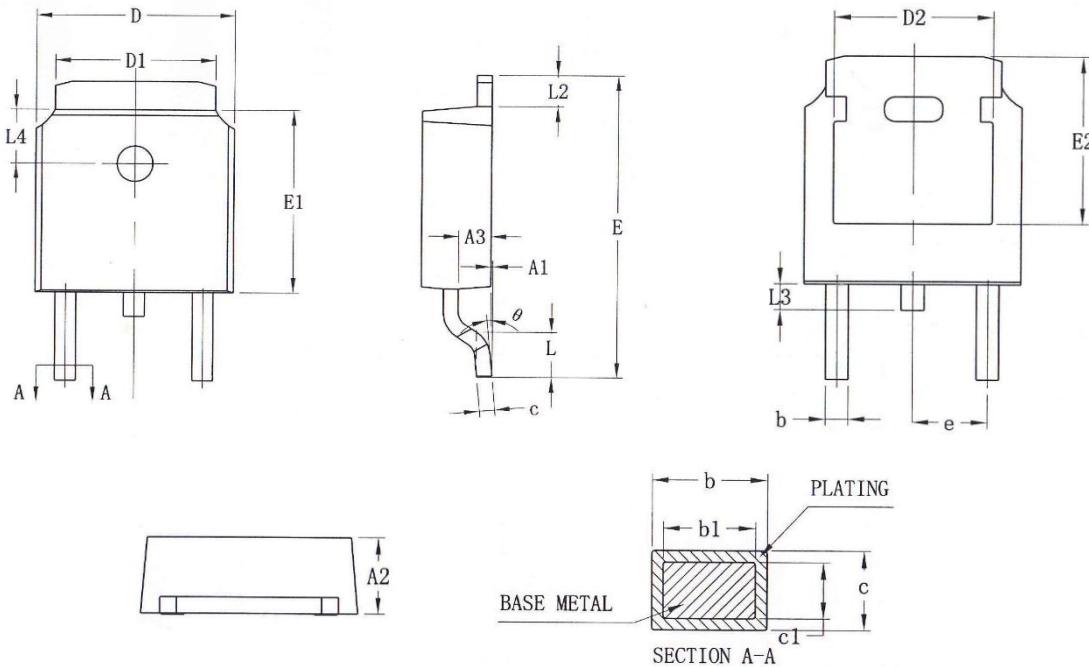
Power Dissipation

■ TYPICAL CHARACTERISTICS



Gate Charge Waveform



TO-252 PACKAGE DIMENSIONS


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A1	0.000	0.100	0.000	0.004
A2	2.200	2.400	0.087	0.094
A3	1.020	1.120	0.040	0.044
b	0.740	0.820	0.029	0.032
b1	0.730	0.790	0.029	0.031
c	0.510	0.550	0.020	0.022
c1	0.500	0.520	0.019	0.020
D	6.500	6.700	0.256	0.264
D1	5.330 REF.		0.210 REF.	
D2	4.830 REF.		0.190 REF.	
E	9.900	10.30	0.390	0.406
E1	6.000	6.200	0.236	0.244
E2	5.300 REF.		0.209 REF.	
e	2.286 BSC.		0.090 BSC.	
L	1.400	1.600	0.055	0.063
L2	0.900	1.250	0.035	0.049
L3	0.600	1.000	0.024	0.039
L4	1.700	1.900	0.067	0.075
theta	0°	8°	0°	15°

Recommended Land Pattern

