

## Single P-Channel MOSFET

### DESCRIPTION

SMC9435M is the P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior fast switching performance. These devices are well suited for high efficiency fast switching applications.

### PART NUMBER INFORMATION

**SMC 9435 M - TR G**  
 a    b    c    d    e

- a : Company name.
- b : Product Serial number.
- c : Package code            M:SOP-8
- d : Handling code            TR:Tape&Reel
- e : Green produce code    G:RoHS Compliant

### FEATURES

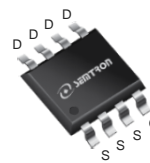
**$V_{DS}=-30V$ ,  $I_D=-6.5A$**

$R_{DS(ON)}=40m\Omega(Typ.) @V_{GS}=-10V$   
 $R_{DS(ON)}=54m\Omega(Typ.) @V_{GS}=-4.5V$

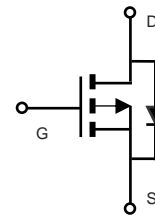
- ◆Fast switch
- ◆Low gate charge
- ◆High power and current handling capability

### APPLICATIONS

- ◆Load Switch
- ◆Portable Equipment
- ◆DC-DC Power Management



SOP-8



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DSS}$	Drain-Source Voltage	-30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_A=25^\circ C$	-6.5
		$T_A=70^\circ C$	-5.2
$I_{DM}$	Pulsed Drain Current <sup>B</sup>	-26	A
$I_{AS}$	Avalanche Current <sup>B</sup>	-20	A
$E_{AS}$	Single Pulse Avalanche energy $L=0.3mH$ <sup>B</sup>	60	mJ
$P_D$	Power Dissipation <sup>A</sup>	$T_A=25^\circ C$	3.1
		$T_A=70^\circ C$	2
$T_J$	Operation Junction Temperature	-55/150	$^\circ C$
$T_{STG}$	Storage Temperature Range	-55/150	$^\circ C$

### THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>A</sup>	$t \leq 10s$	40	$^\circ C/W$
	Thermal Resistance Junction to Ambient <sup>AC</sup>	Steady-State	80	
$R_{\theta JC}$	Thermal Resistance Junction to Case		30	

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ Unless otherwise noted)

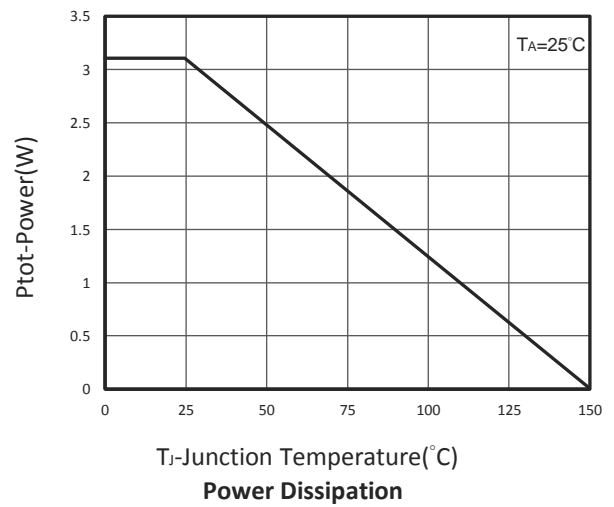
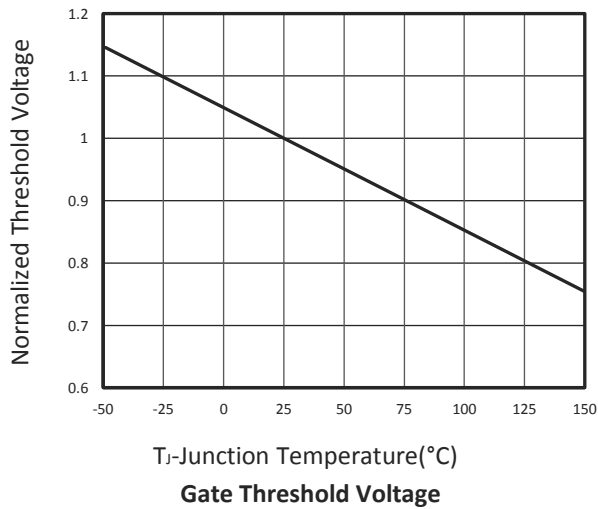
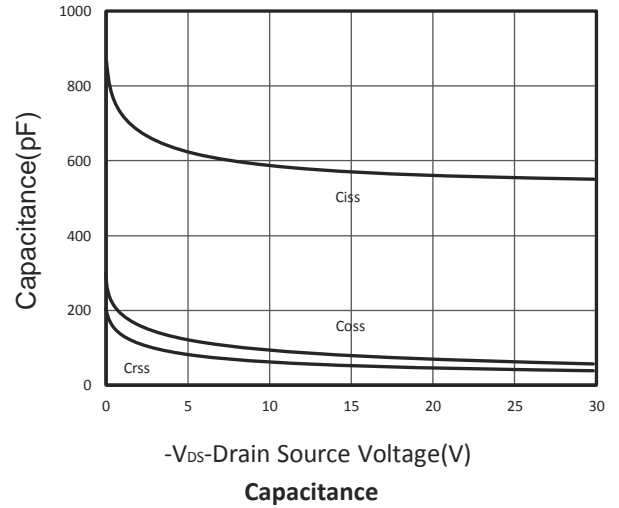
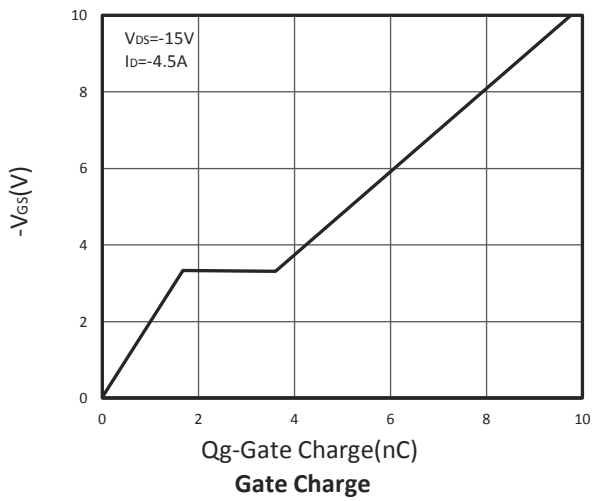
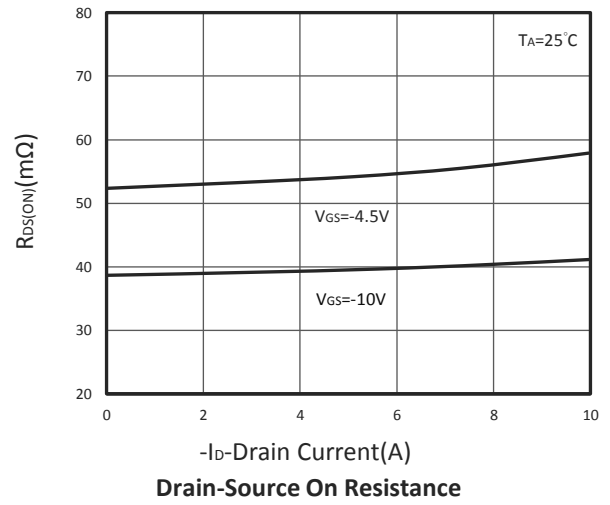
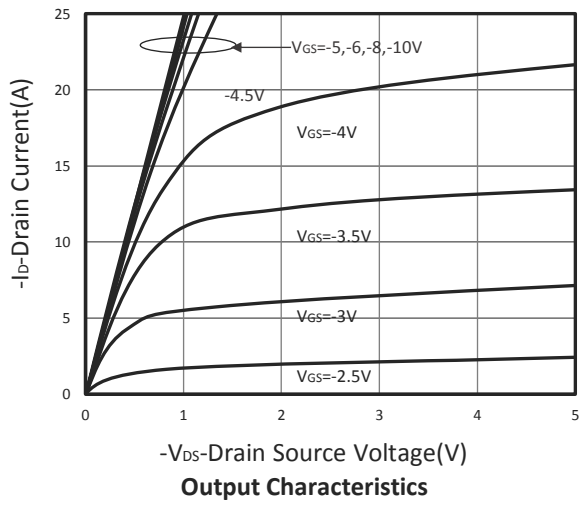
Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Static Parameters</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250 $\mu$ A	-30			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250 $\mu$ A	-1	-1.5	-2	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = $\pm$ 20V			$\pm$ 100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V, T <sub>J</sub> =25 $^\circ$ C			-1	$\mu$ A
		V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V, T <sub>J</sub> =75 $^\circ$ C			-10	
R <sub>DS(ON)</sub>	Drain-source On-Resistance <sup>D</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-6.5A V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A		40 54	48 65	m $\Omega$
G <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =-10V, I <sub>D</sub> =-4.5A		12		S
<b>Diode Characteristics</b>						
V <sub>SD</sub>	Diode Forward Voltage <sup>D</sup>	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V			-1	V
I <sub>S</sub>	Diode Continuous Forward Current				-6.4	A
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =-4.5A, di/dt=100A/ $\mu$ s		15		ns
Q <sub>rr</sub>	Reverse Recovery Charge	T <sub>J</sub> =25 $^\circ$ C		9.8		nC
<b>Dynamic and Switching Parameters<sup>E</sup></b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-15V, V <sub>GS</sub> =-10V I <sub>D</sub> =-4.5A		9.8	13.8	nC
Q <sub>g</sub>	Total Gate Charge (4.5V)			4.8	6.7	
Q <sub>gs</sub>	Gate-Source Charge			1.7	2.4	
Q <sub>gd</sub>	Gate-Drain Charge			2	2.8	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz		580		pF
C <sub>oss</sub>	Output Capacitance			68		
C <sub>rss</sub>	Reverse Transfer Capacitance			58		
t <sub>d(on)</sub>	Turn-On Time <sup>D</sup>	V <sub>DD</sub> =-15V, V <sub>GEN</sub> =-10V R <sub>G</sub> =6 $\Omega$ , I <sub>D</sub> =-1A		8.3		nS
t <sub>r</sub>				10		
t <sub>d(off)</sub>	Turn-Off Time <sup>D</sup>			16.8		
t <sub>f</sub>				7.8		

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

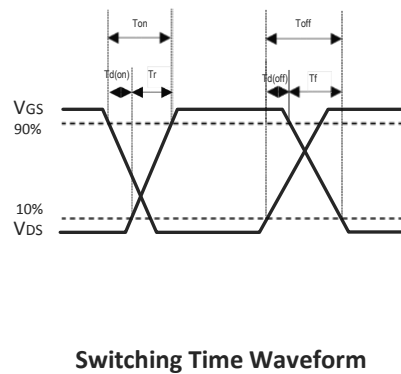
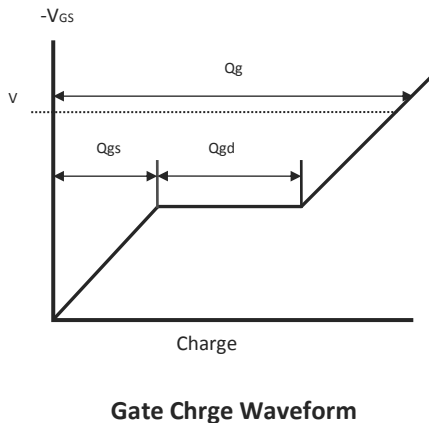
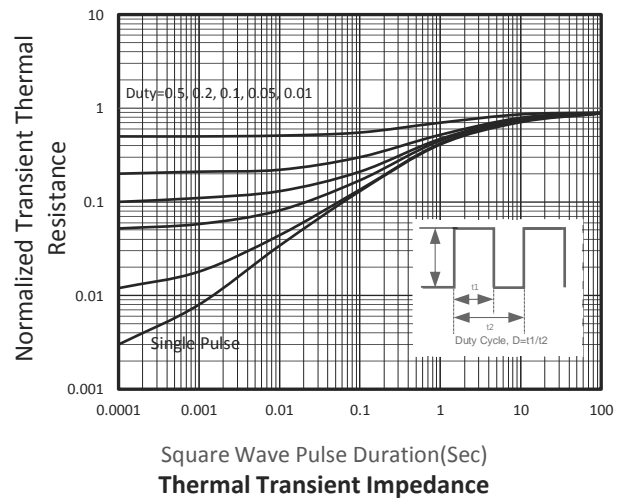
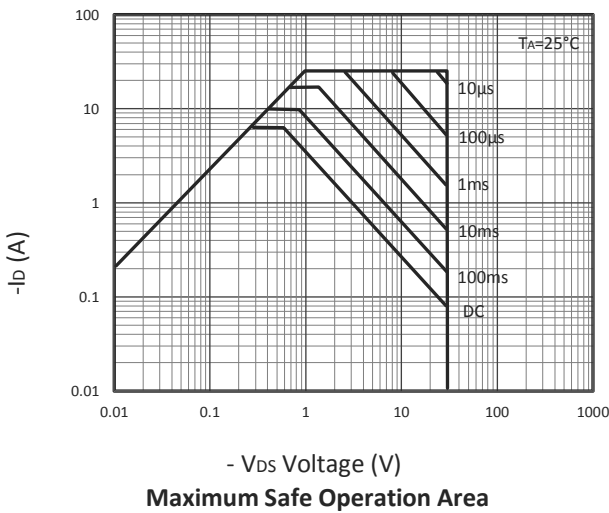
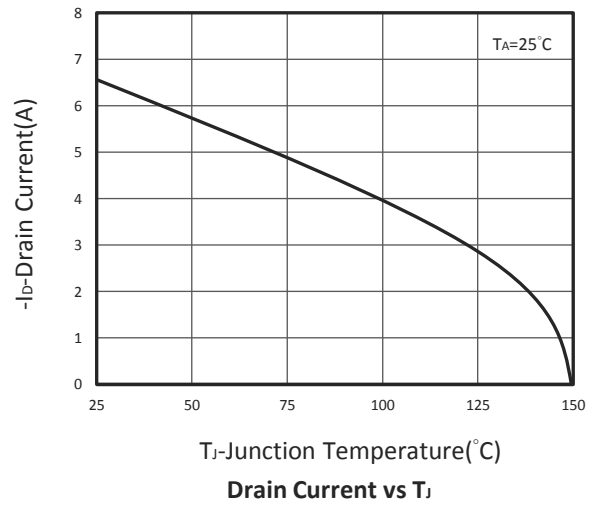
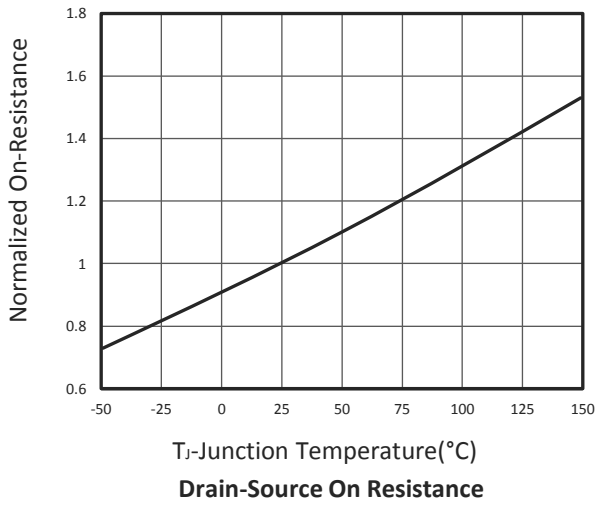
- A. Surface mounted on FR4 board using 1 in<sup>2</sup> pad size.
- B. Pulsed width limited by maximum junction temperature, T<sub>J(MAX)</sub>=150 $^\circ$ C (initial temperature T<sub>J</sub>=25 $^\circ$ C).
- C. Using  $\leq$  10s junction-to-ambient thermal resistance is base on T<sub>J(MAX)</sub>=150 $^\circ$ C.
- D. Pulse test width  $\leq$ 300 $\mu$ s and duty cycle  $\leq$  2%.
- E. Guaranteed by design, not subject to production testing.

The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date. We assume no responsibility for any infringement of patents, patent rights, or other rights arising from the use of any information and circuitry in this datasheet.

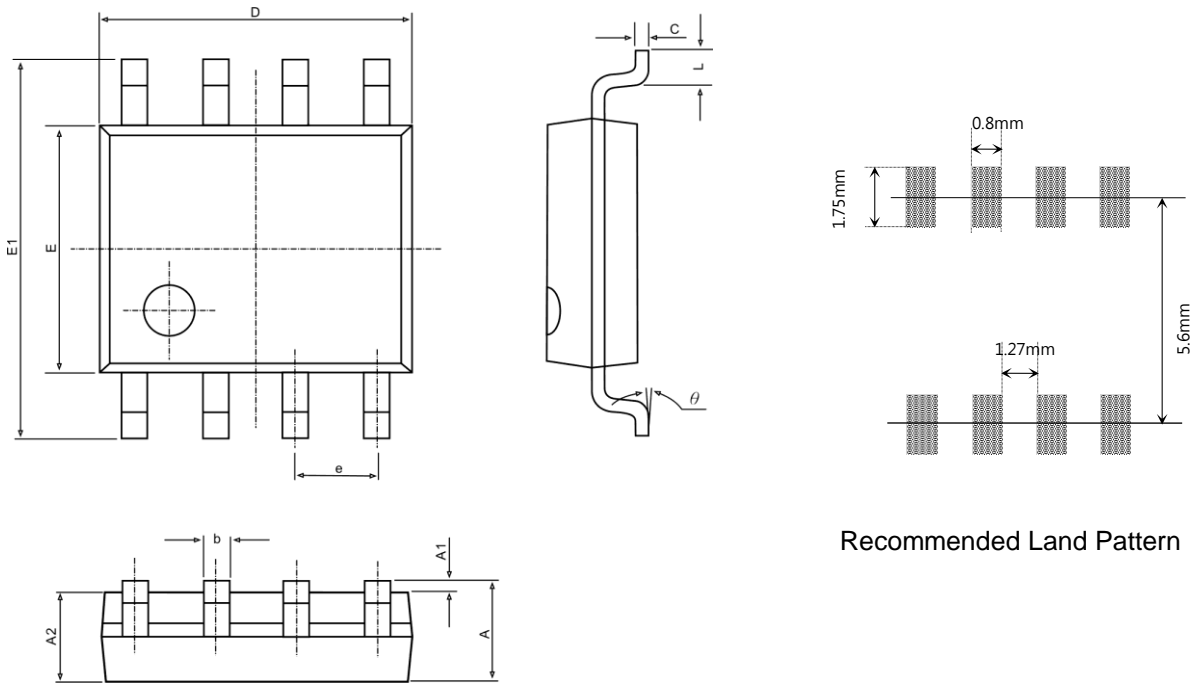
**TYPICAL CHARACTERISTICS**



## TYPICAL CHARACTERISTICS



## ■ SOP-8 PACKAGE DIMENSIONS



Recommended Land Pattern

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.040.	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.130	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270BSC.		0.050BSC.	
L	0.400	1.270	0.016	0.005
θ	0°	8°	0°	8°