

Single N-Channel MOSFET

DESCRIPTION

SMC4458M is the N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior, fast switching performance. These devices are well suited for high efficiency fast switching applications.

PART NUMBER INFORMATION

SMC 4458 M - TR G
 a b c d e

- a : Company name.
- b : Product Serial number.
- c : Package code M:SOP-8
- d : Handling code TR:Tape&Reel
- e : Green produce code G:RoHS Compliant

FEATURES

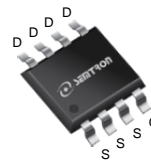
$V_{DS}=40V, I_D=12.5A$

$R_{DS(ON)}=10m\Omega(Typ.)@V_{GS}=10V$
 $R_{DS(ON)}=14m\Omega(Typ.)@V_{GS}=4.5V$

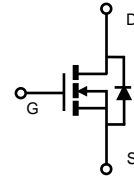
- ◆ 100% EAS Guaranteed
- ◆ Low Gate Charge
- ◆ Improved dv/dt Capability

APPLICATIONS

- ◆ Power Management
- ◆ DC/DC Power System



SOP-8



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ C$ Unless otherwise noted)

| Symbol | Parameter | Rating | Units |
|-----------|--|------------------|------------|
| V_{DSS} | Drain-Source Voltage | 40 | V |
| V_{GSS} | Gate-Source Voltage | ± 20 | V |
| I_D | Continuous Drain Current | $T_A=25^\circ C$ | 12.5 |
| | | $T_A=70^\circ C$ | 9.9 |
| I_{DM} | Pulsed Drain Current ^B | 50 | A |
| I_{AS} | Avalanche Current ^B | 30 | A |
| EAS | Single Pulse Avalanche energy $L=0.1mH$ ^B | 45 | mJ |
| P_D | Power Dissipation ^A | $T_A=25^\circ C$ | 3.1 |
| | | $T_A=70^\circ C$ | 2 |
| T_J | Operation Junction Temperature | -55/150 | $^\circ C$ |
| T_{STG} | Storage Temperature Range | -55/150 | $^\circ C$ |

THERMAL RESISTANCE

| Symbol | Parameter | Typ | Max | Units |
|-----------------|--|--------------|-----|--------------|
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient ^A | | 40 | $^\circ C/W$ |
| | Thermal Resistance Junction to Ambient ^{AC} | $t \leq 10s$ | 70 | |
| $R_{\theta JC}$ | Thermal Resistance Junction to Case | Steady-State | 25 | |

ELECTRICAL CHARACTERISTICS (T_A=25°C Unless otherwise noted)

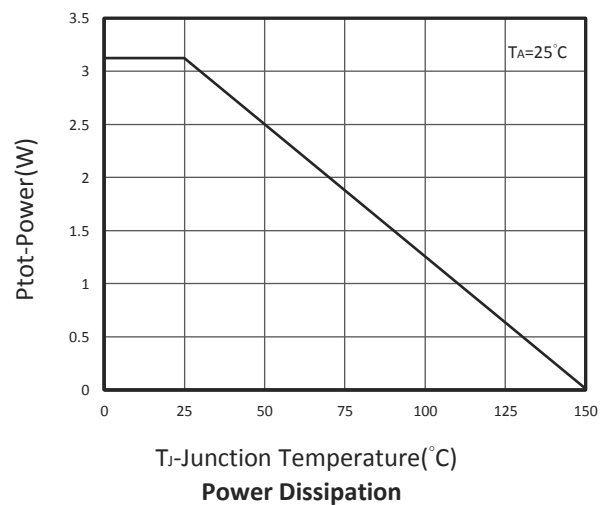
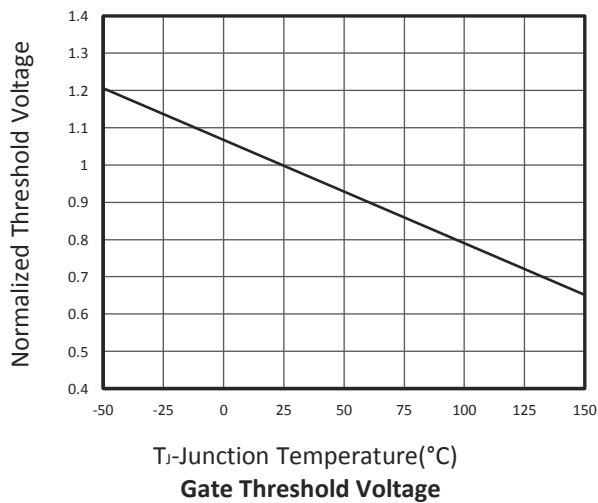
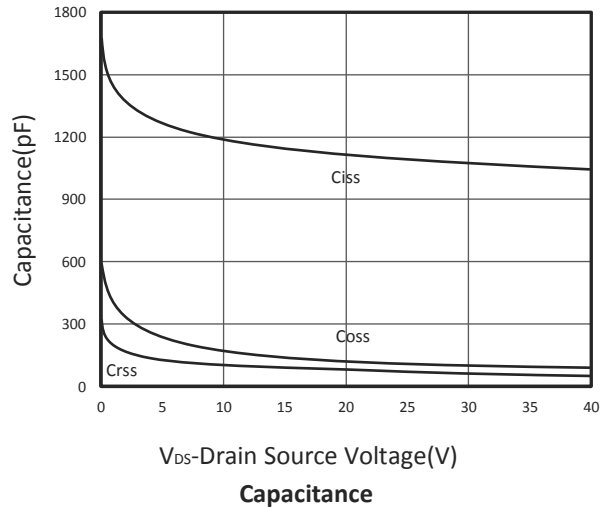
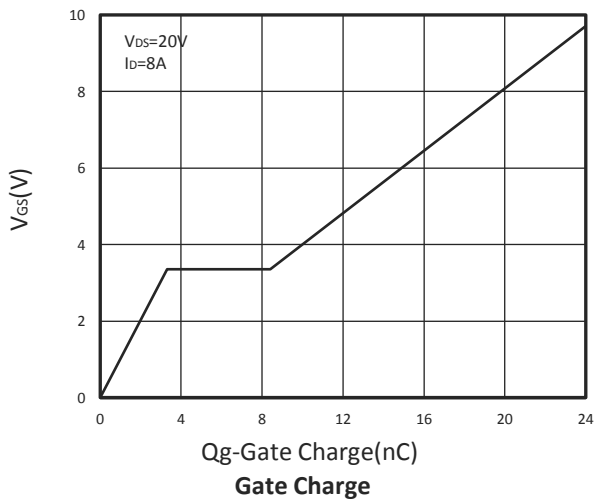
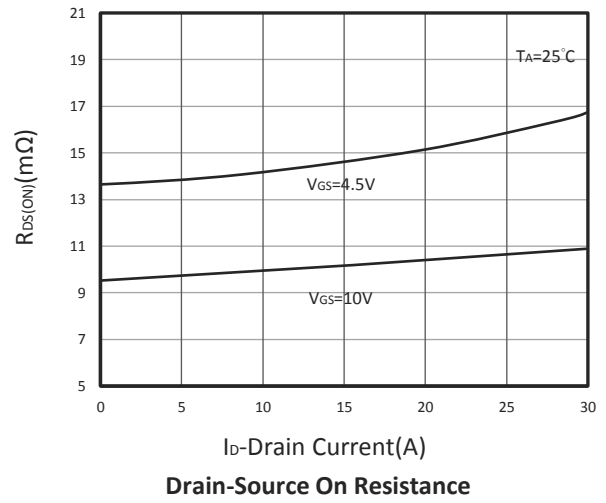
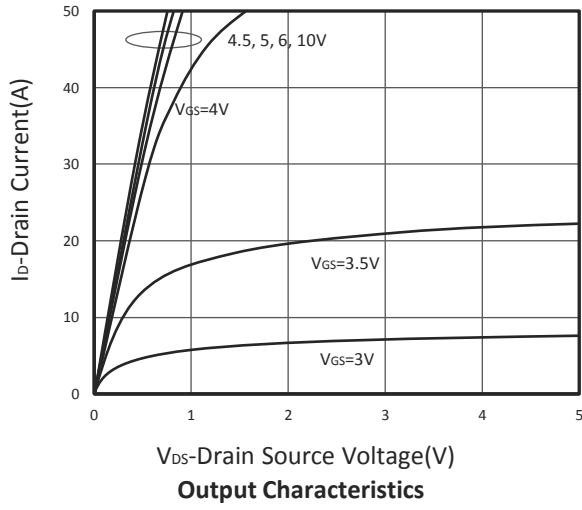
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--|---|--|-----|----------|----------|------|
| Static Parameters | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | V _{GS} =0V, I _D =250μA | 30 | | | V |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250μA | 1.2 | 1.7 | 2.5 | V |
| I _{GSS} | Gate Leakage Current | V _{DS} =0V, V _{GS} =±20V | | | ±100 | nA |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =40V, V _{GS} =0V, T _J =25°C | | | 1 | μA |
| | | V _{DS} =32V, V _{GS} =0V, T _J =75°C | | | 10 | |
| R _{DS(ON)} | Drain-source On-Resistance ^D | V _{GS} =10V, I _D =12.5A V _{GS} =4.5V, I _D =8A | | 10 14 | 12 17 | mΩ |
| G _{fs} | Forward Transconductance | V _{DS} =5V, I _D =8A | | 33 | | S |
| Diode Characteristics | | | | | | |
| V _{SD} | Diode Forward Voltage ^D | I _S =1A, V _{GS} =0V | | | 1.0 | V |
| I _S | Diode Continuous Forward Current | | | | 12.5 | A |
| t _{rr} | Reverse Recovery Time | I _S =8A, di/dt=100A/μs | | 10 | | ns |
| Q _{rr} | Reverse Recovery Charge | | | 3.5 | | nC |
| Dynamic and Switching Parameters ^E | | | | | | |
| Q _g | Total Gate Charge | V _{DS} =20V, V _{GS} =10V, I _D =8A | | 24.8 | 30.1 | nC |
| Q _g | Total Gate Charge (4.5V) | | | 11.8 | 13.9 | |
| Q _{gs} | Gate-Source Charge | | | 3.6 | 4.3 | |
| Q _{gd} | Gate-Drain Charge | | | 4.7 | 6.6 | |
| C _{iss} | Input Capacitance | V _{DS} =20V, V _{GS} =0V, f=1MHz | | 1110 | 1430 | pF |
| C _{oss} | Output Capacitance | | | 108 | 141 | |
| C _{rss} | Reverse Transfer Capacitance | | | 82 | 115 | |
| R _g | Gate Resistance | V _{GS} =0V, V _{DS} =0V, F=1MHz | | 2.5 | | Ω |
| t _{d(on)} | Turn-On Time | V _{DD} =20V, V _{GEN} =10V R _G =3.3Ω, I _D =1A | | 7.8 | 16 | nS |
| t _r | | | | 3 | 6 | |
| t _{d(off)} | Turn-Off Time | | | 28 | 49 | |
| t _f | | | | 3.1 | 5.9 | |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

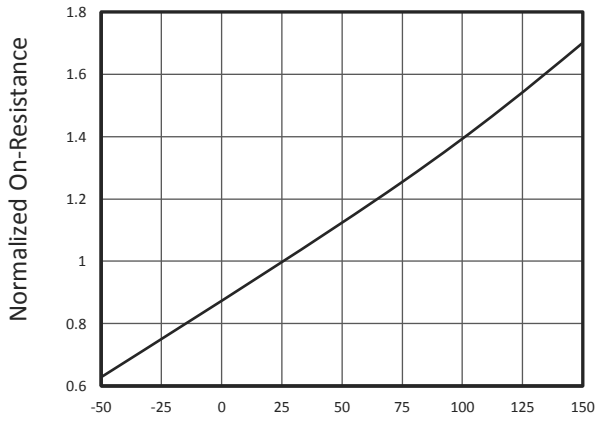
- A. Surface mounted on FR4 board using 1 in² pad size.
- B. Pulsed width limited by maximum junction temperature, T_{J(MAX)}=150°C (initial temperature T_J=25°C).
- C. Using ≤ 10s junction-to-ambient thermal resistance is base on T_{J(MAX)}=150°C.
- D. Pulse test width ≤300μs and duty cycle ≤ 2%.
- E. Guaranteed by design, not subject to production testing.

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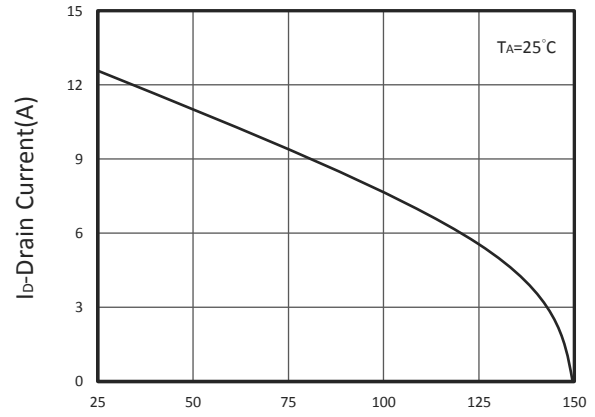
TYPICAL CHARACTERISTICS



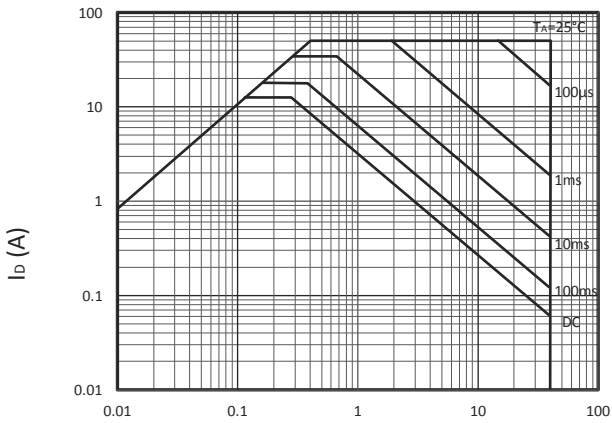
TYPICAL CHARACTERISTICS



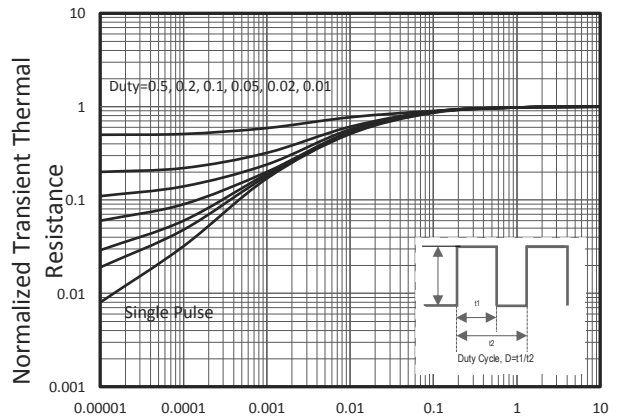
T_J-Junction Temperature(°C)
Drain-Source On Resistance



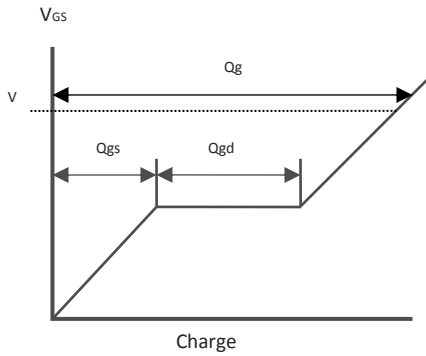
T_J-Junction Temperature(°C)
Drain Current vs T_J



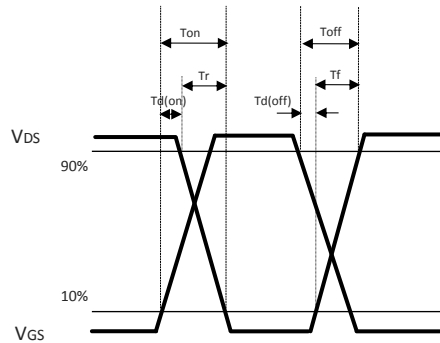
V_{DS} Voltage (V)
Maximum Safe Operation Area



Square Wave Pulse Duration(Sec)
Thermal Transient Impedance

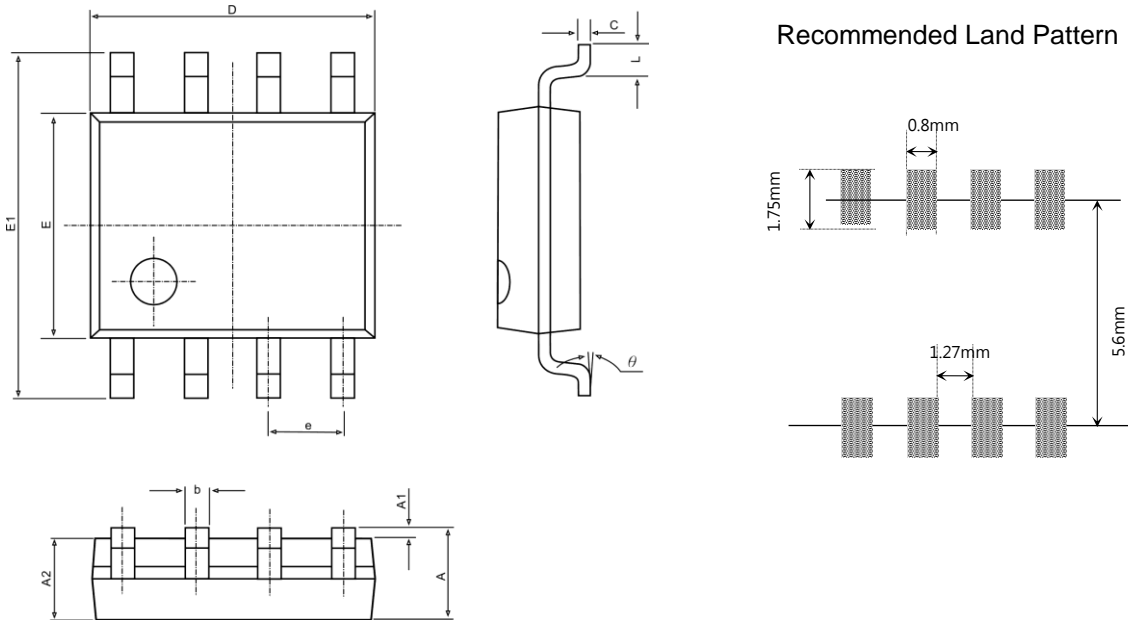


Gate Chrg Waveform



Switching Time Waveform

■ SOP-8 PACKAGE DIMENSIONS



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min. | Max. | Min. | Max. |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.300 | 1.500 | 0.051 | 0.059 |
| b | 0.390 | 0.490 | 0.015 | 0.019 |
| c | 0.200 | 0.250 | 0.008 | 0.010 |
| D | 4.800 | 5.100 | 0.189 | 0.201 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270 BSC | | 0.050 BSC | |
| L | 0.500 | 0.800 | 0.020 | 0.031 |
| θ | 0° | 8° | 0° | 8° |