

## Single N-Channel MOSFET

### DESCRIPTION

SMC4428M is the N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior, fast switching performance. These devices are well suited for high efficiency fast switching applications.

### PART NUMBER INFORMATION

**SMC 4428 M - TR G**  
 a      b      c      d      e

- a : Company name.
- b : Product Serial number.
- c : Package code            M:SOP-8
- d : Handling code            TR:Tape&Reel
- e : Green produce code    G:RoHS Compliant

### FEATURES

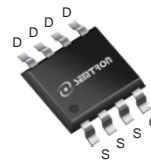
**$V_{DS}=30V, I_D=16A$**

$R_{DS(ON)}=5.5m\Omega(Typ.)@V_{GS}=10V$   
 $R_{DS(ON)}=7.0m\Omega(Typ.)@V_{GS}=4.5V$

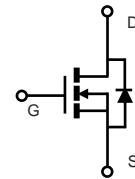
- ◆ 100% EAS Guaranteed
- ◆ Improved dv/dt capability
- ◆ High power and current handling capability

### APPLICATIONS

- ◆ Power Management
- ◆ DC/DC Power System
- ◆ Load Switch



SOP-8



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_A=25^\circ C$	16
		$T_A=70^\circ C$	13
$I_{DM}$	Pulsed Drain Current <sup>B</sup>	64	A
$I_{AS}$	Avalanche Current <sup>B</sup>	30	A
EAS	Single Pulse Avalanche energy $L=0.1mH$ <sup>B</sup>	45	mJ
$P_D$	Power Dissipation <sup>A</sup>	$T_A=25^\circ C$	3.1
		$T_A=70^\circ C$	2
$T_J$	Operation Junction Temperature	-55/150	$^\circ C$
$T_{STG}$	Storage Temperature Range	-55/150	$^\circ C$

### THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>A</sup>		40	$^\circ C/W$
	Thermal Resistance Junction to Ambient <sup>AC</sup>	$t \leq 10s$	75	
$R_{\theta JC}$	Thermal Resistance Junction to Case	Steady-State	21	

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ Unless otherwise noted)

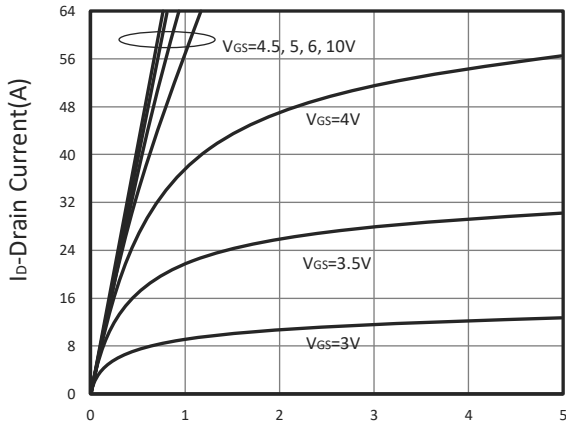
Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Static Parameters</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 $\mu$ A	30			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 $\mu$ A	1	1.6	2.5	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = $\pm$ 20V			$\pm$ 100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, T <sub>J</sub> =25 $^\circ$ C			1	$\mu$ A
		V <sub>DS</sub> =24V, V <sub>GS</sub> =0V, T <sub>J</sub> =75 $^\circ$ C			10	
R <sub>DS(ON)</sub>	Drain-source On-Resistance <sup>D</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =16A V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A		5.5 7	7 10	m $\Omega$
G <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =10A		62		S
<b>Diode Characteristics</b>						
V <sub>SD</sub>	Diode Forward Voltage <sup>D</sup>	I <sub>S</sub> =1A, V <sub>GS</sub> =0V			1	V
I <sub>S</sub>	Diode Continuous Forward Current				8	A
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =10A, di/dt=100A/ $\mu$ s		25		ns
Q <sub>rr</sub>	Reverse Recovery Charge			12		nC
<b>Dynamic and Switching Parameters <sup>E</sup></b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V, V <sub>GS</sub> =10V, I <sub>D</sub> =10A		19.7	27.6	nC
Q <sub>g</sub>	Total Gate Charge (4.5V)			9.6	12	
Q <sub>gs</sub>	Gate-Source Charge			5	6.3	
Q <sub>gd</sub>	Gate-Drain Charge			3.8	5.1	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz		1750		pF
C <sub>oss</sub>	Output Capacitance			267		
C <sub>rss</sub>	Reverse Transfer Capacitance			168		
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, F=1MHz		2.2		$\Omega$
t <sub>d(on)</sub>	Turn-On Time	V <sub>DD</sub> =15V, V <sub>GEN</sub> =10V R <sub>G</sub> =6 $\Omega$ , I <sub>D</sub> =1A		9	17	nS
t <sub>r</sub>				6	12	
t <sub>d(off)</sub>	Turn-Off Time			32.4	62	
t <sub>f</sub>				9.2	17	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

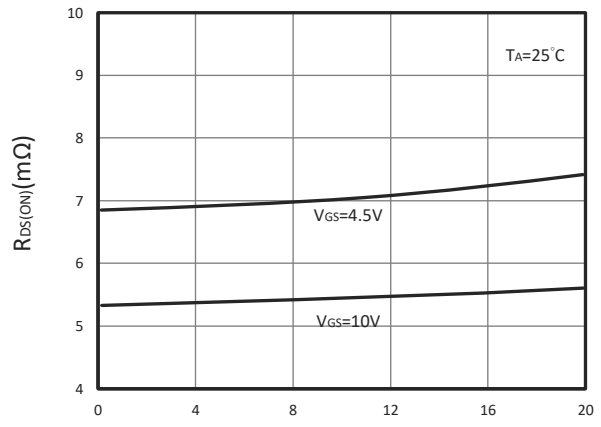
- A. Surface mounted on FR4 board using 1 in<sup>2</sup> pad size.
- B. Pulsed width limited by maximum junction temperature, T<sub>J(MAX)</sub>=150 $^\circ$ C.
- C. Using  $\leq$  10s junction-to-ambient thermal resistance is base on T<sub>J(MAX)</sub>=150 $^\circ$ C.
- D. Pulse test width  $\leq$ 300 $\mu$ s and duty cycle  $\leq$  2%.
- E. Guaranteed by design, not subject to production testing.

The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date. We assume no responsibility for any infringement of patents, patent rights, or other rights arising from the use of any information and circuitry in this datasheet.

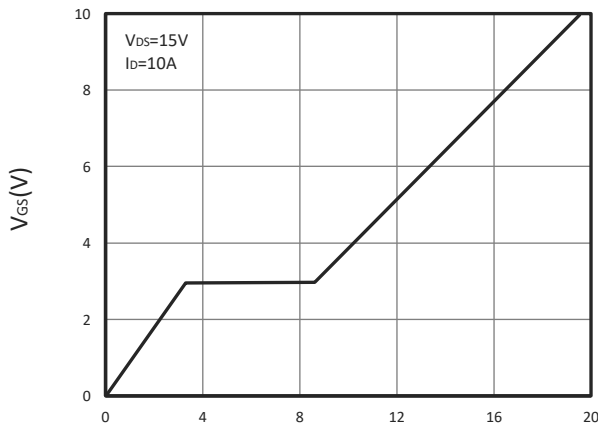
**TYPICAL CHARACTERISTICS**



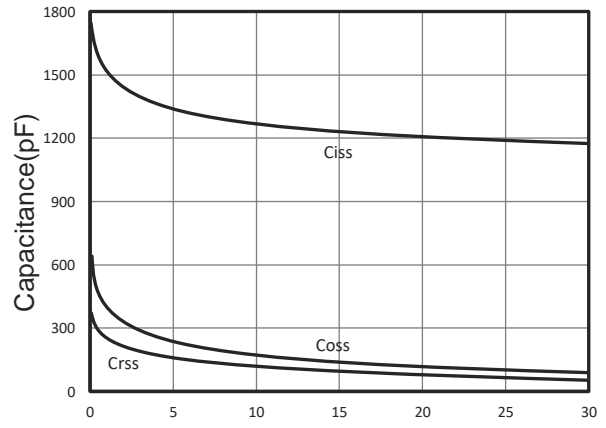
**Output Characteristics**



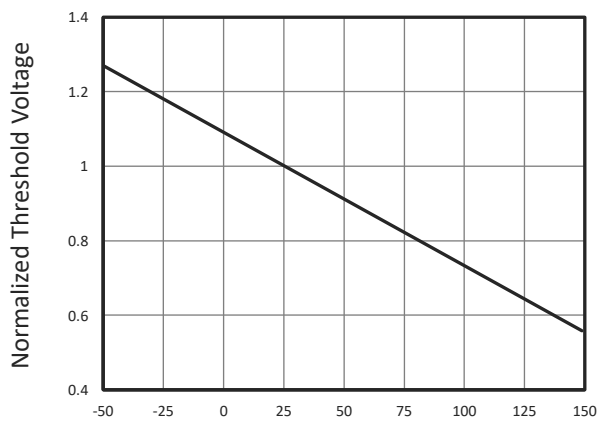
**Drain-Source On Resistance**



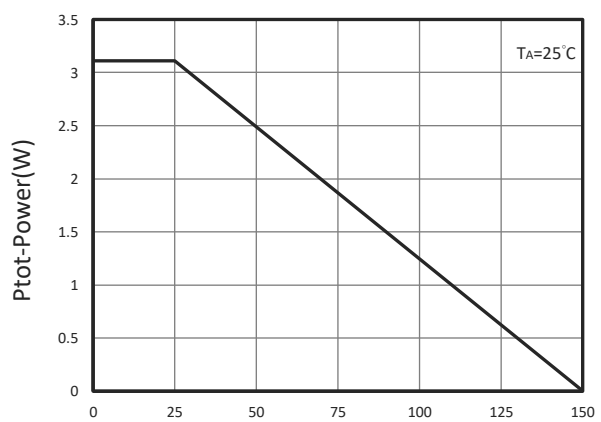
**Gate Charge**



**Capacitance**

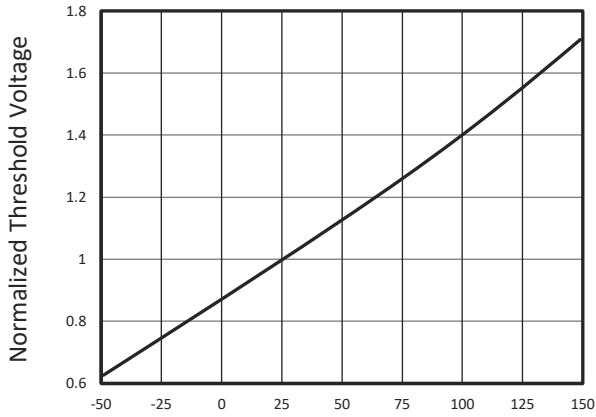


**Gate Threshold Voltage**

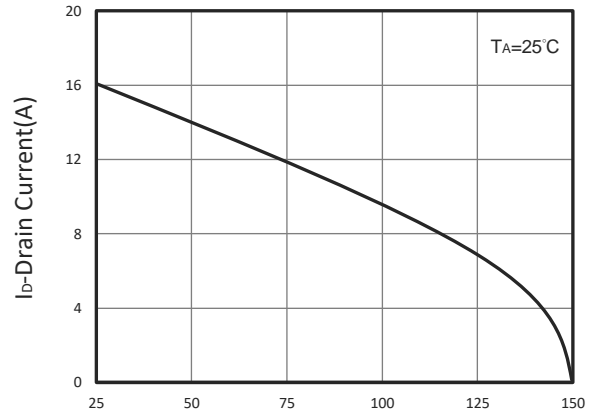


**Power Dissipation**

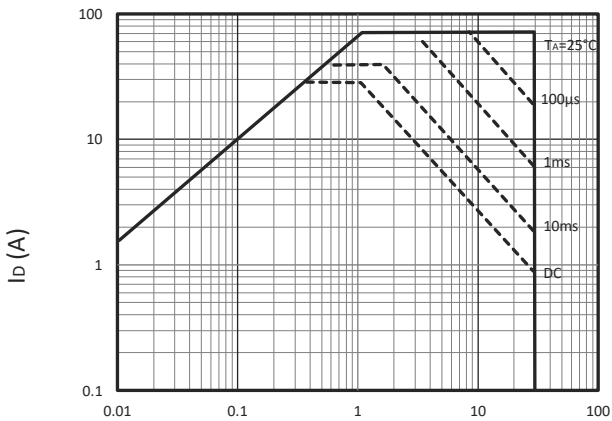
## TYPICAL CHARACTERISTICS



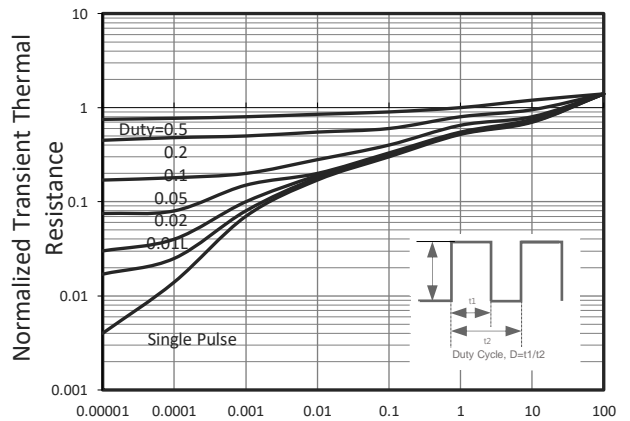
T<sub>J</sub>-Junction Temperature(°C)  
Gate Threshold Voltage



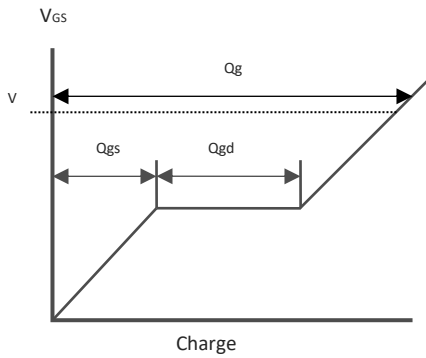
T<sub>J</sub>-Junction Temperature(°C)  
Drain Current vs T<sub>J</sub>



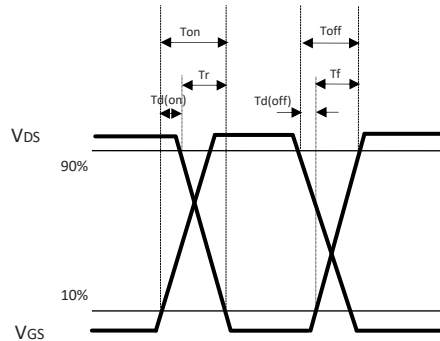
V<sub>ds</sub> Voltage (V)  
Maximum Safe Operation Area



Square Wave Pulse Duration(Sec)  
Thermal Transient Impedance

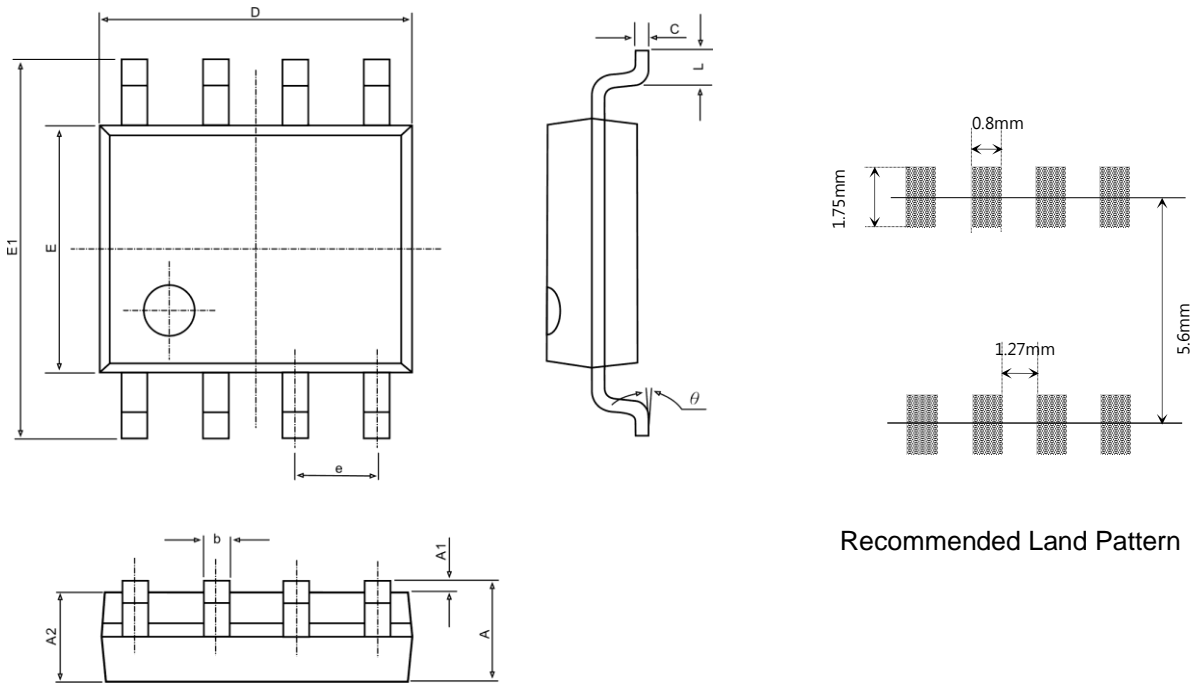


Gate Chrg Waveform



Switching Time Waveform

## ■ SOP-8 PACKAGE DIMENSIONS



Recommended Land Pattern

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.040	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.130	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270BSC.		0.050BSC.	
L	0.400	1.270	0.016	0.005
θ	0°	8°	0°	8°