

Single P-Channel MOSFET

DESCRIPTION

SMC4239M is the P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior, fast switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

PART NUMBER INFORMATION

SMC 4239 M - TR G
 a b c d e

- a : Company name.
- b : Product Serial number.
- c : Package code M:SOP-8
- d : Handling code TR:Tape&Reel
- e : Green produce code G:RoHS Compliant

FEATURES

$V_{DS}=-40V$, $I_D=-11A$

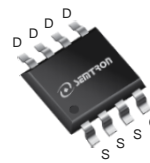
$R_{DS(ON)}=12.5m\Omega(Typ.)@V_{GS}=-10V$

$R_{DS(ON)}=16m\Omega(Typ.)@V_{GS}=-4.5V$

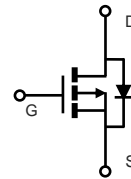
- ◆ 100% EAS Guarantee
- ◆ High power and current handling capability

APPLICATIONS

- ◆ Load Switch
- ◆ Power Management
- ◆ Motor Drives



SOP-8



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-Source Voltage	-40	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_A=25^\circ C$	-11
		$T_A=70^\circ C$	-8.8
I_{DM}	Pulsed Drain Current ^B	-44	A
I_{AS}	Avalanche Current ^B	-30	A
EAS	Single Pulse Avalanche energy $L=0.1mH$ ^B	45	mJ
P_D	Power Dissipation ^A	$T_A=25^\circ C$	3.1
		$T_A=70^\circ C$	2
T_J	Operation Junction Temperature	-55/150	$^\circ C$
T_{STG}	Storage Temperature Range	-55/150	$^\circ C$

THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^A	$t \leq 10s$	40	$^\circ C/W$
	Thermal Resistance Junction to Ambient ^{AC}	Steady-State	70	

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

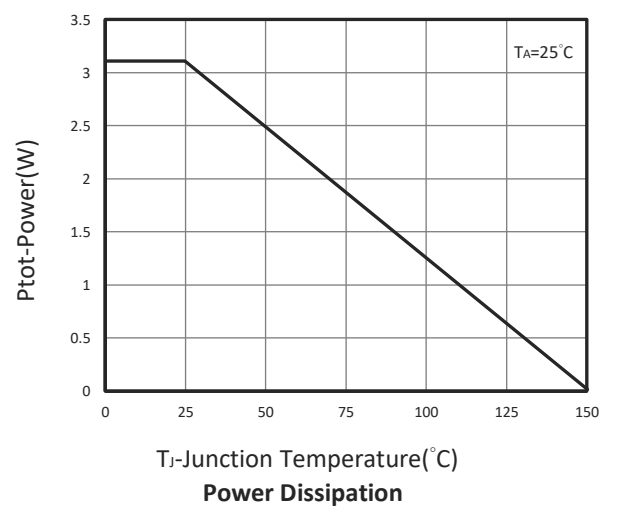
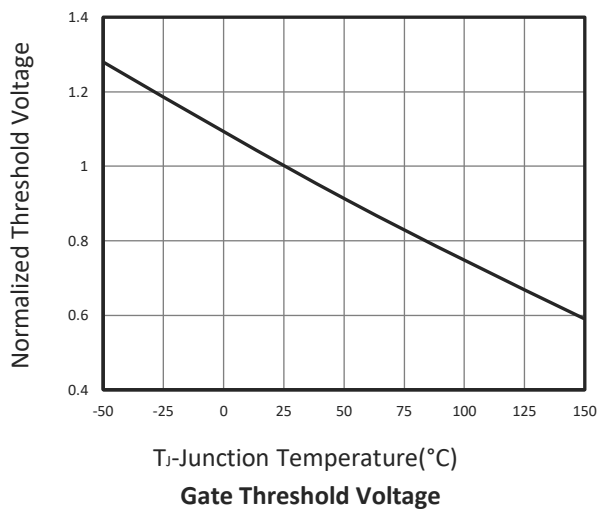
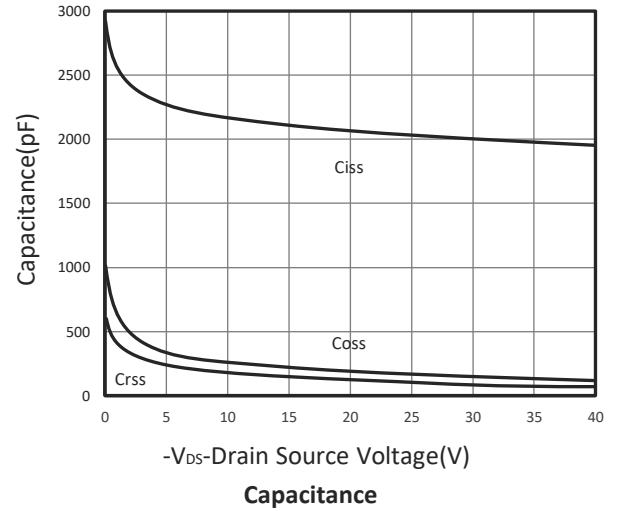
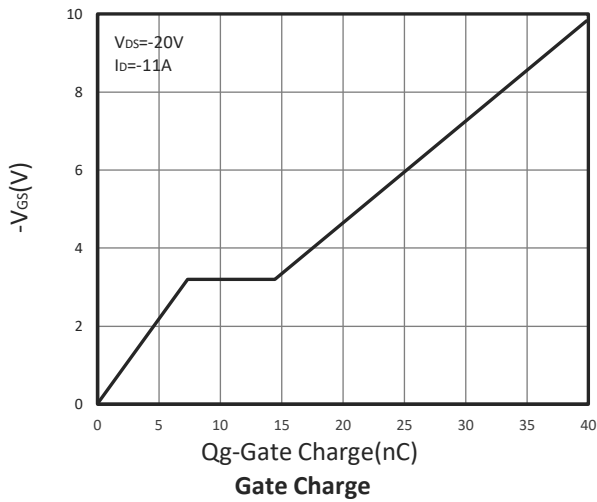
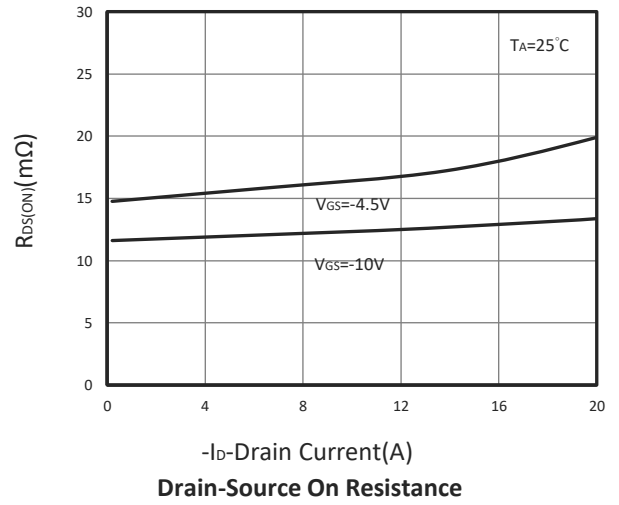
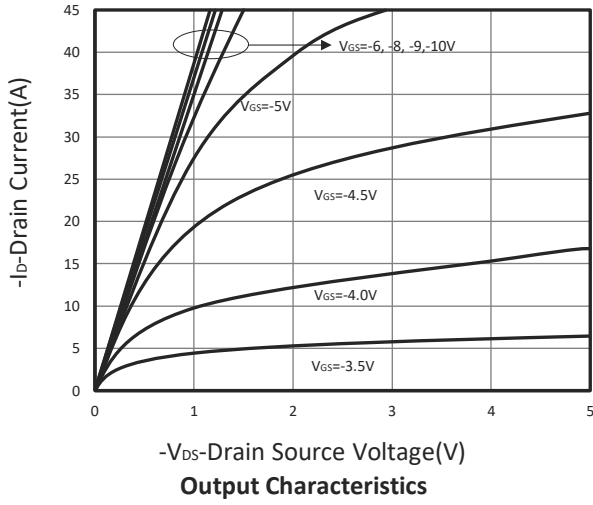
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μ A	-40			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μ A	-1	-1.6	-2.5	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} = \pm 20V			\pm 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-40V, V _{GS} =0V, T _J =25 $^\circ$ C			-1	μ A
		V _{DS} =-32V, V _{GS} =0V, T _J =75 $^\circ$ C			-10	
R _{DS(ON)}	Drain-source On-Resistance ^D	V _{GS} =-10V, I _D =-11A V _{GS} =-4.5V, I _D =-8A		12.5 16	15 20	m Ω
G _{fs}	Forward Transconductance	V _{DS} =-10V, I _D =-11A		30		S
Diode Characteristics						
V _{SD}	Diode Forward Voltage ^D	I _S =-1A, V _{GS} =0V			-1	V
I _S	Continuous Source Current				-5.5	A
t _{rr}	Reverse Recovery Time	I _S =-11A, di/dt=100A/ μ s		28		ns
Q _{rr}	Reverse Recovery Charge			21		nC
Dynamic and Switching Parameters^E						
Q _g	Total Gate Charge	V _{DS} =-20V, V _{GS} =-10V I _D =-11A		40.6	54.8	nC
Q _g	Total Gate Charge (4.5V)			19.8	26.7	
Q _{gs}	Gate-Source Charge			6.8	9.2	
Q _{gd}	Gate-Drain Charge			7.8	10.5	
C _{iss}	Input Capacitance	V _{DS} =-20V, V _{GS} =0V, f=1MHz		2050		pF
C _{oss}	Output Capacitance			175		
C _{rss}	Reverse Transfer Capacitance			126		
R _g	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz		8.5		Ω
t _{d(on)}	Turn-On Time	V _{DD} =-20V, V _{GEN} =-10V R _G =6 Ω I _D =-1A		17.3		nS
t _r				13		
t _{d(off)}	Turn-Off Time			70		
t _f				32		

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

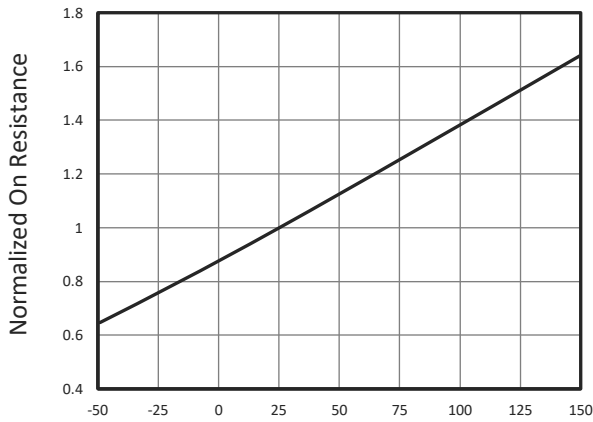
- A. Surface mounted on FR4 board using 1 in² pad size.
- B. Pulsed width limited by maximum junction temperature, T_{J(MAX)}=150 $^\circ$ C.
- C. Using \leq 10s junction-to-ambient thermal resistance is base on T_{J(MAX)}=150 $^\circ$ C.
- D. Pulse test width \leq 300 μ s and duty cycle \leq 2%.
- E. Guaranteed by design, not subject to production testing.

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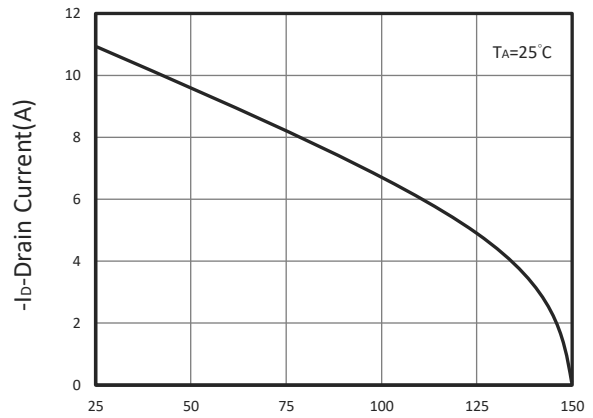
TYPICAL CHARACTERISTICS



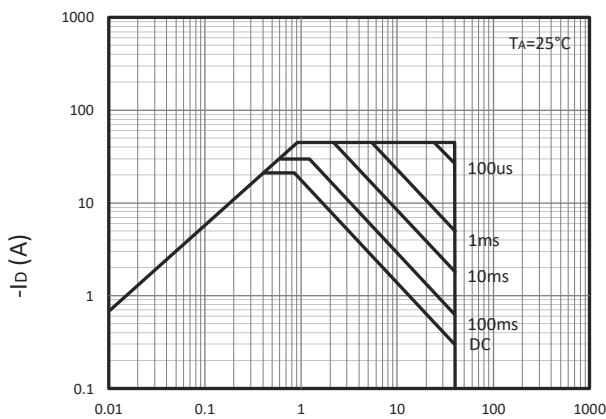
TYPICAL CHARACTERISTICS



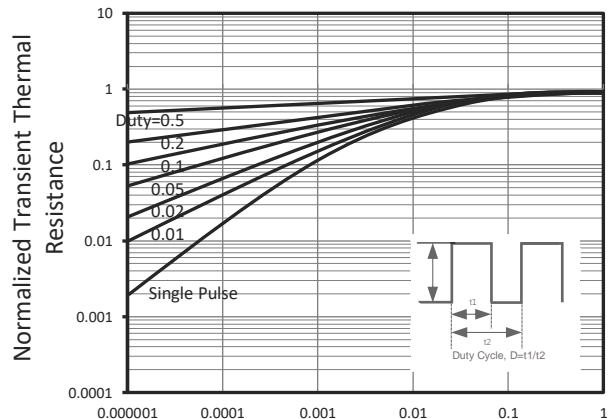
$R_{DS(ON)}$ vs Junction Temperature



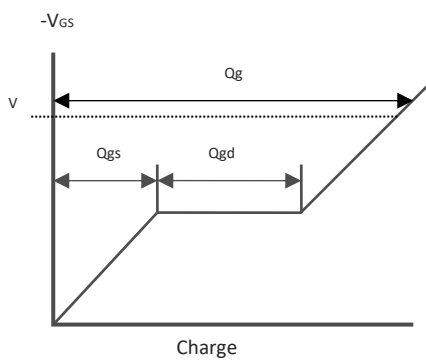
Drain Current vs T_c



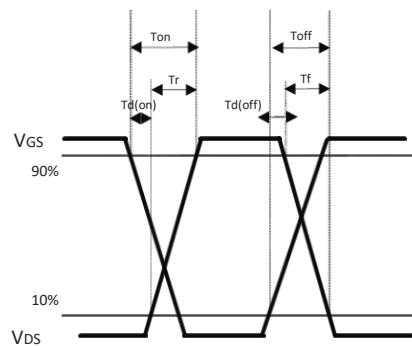
Maximum Safe Operation Area



Thermal Transient Impedance

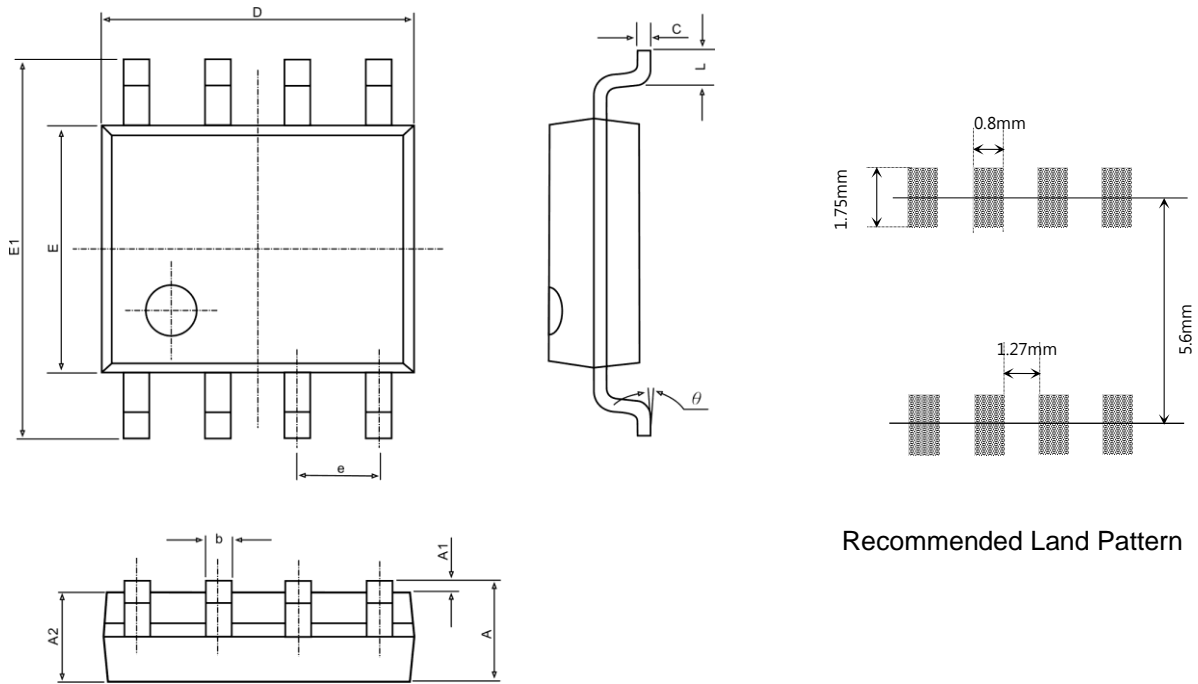


Gate Charge Waveform



Switching Time Waveform

■ SOP-8 PACKAGE DIMENSIONS



Recommended Land Pattern

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.040.	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.130	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270BSC.		0.050BSC.	
L	0.400	1.270	0.016	0.005
θ	0°	8°	0°	8°