

Dual N-Channel MOSFET

DESCRIPTION

SMC4802 is the Dual N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance. This device is ideal for load switch applications.

PART NUMBER INFORMATION

SMC 4802 M - TR G
 a b c d e

- a : Company name.
- b : Product Serial number.
- c : Package code M:SOP-8
- d : Handling code TR:Tape&Reel
- e : Green produce code G:RoHS Compliant

FEATURES

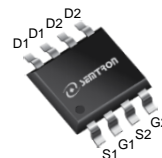
$V_{DS} = 30V, I_D = 12A$

$R_{DS(ON)} = 7m\Omega (Typ.) @ V_{GS} = 10V$
 $R_{DS(ON)} = 8m\Omega (Typ.) @ V_{GS} = 4.5V$

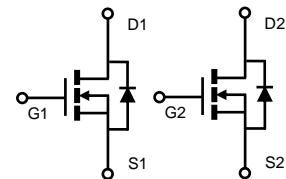
- ◆ 100% EAS Guaranteed
- ◆ Improved dv/dt capability
- ◆ High power and current handling capability

APPLICATIONS

- ◆ Power Management
- ◆ DC/DC Power System
- ◆ Load Switch



SOP-8



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_A = 25^\circ C$	12
		$T_A = 70^\circ C$	9.5
I_{DM}	Pulsed Drain Current ^A	48	A
I_{AS}	Avalanche Current ^A	30	A
EAS	Single Pulse Avalanche energy $L=0.1mH$ ^{AE}	45	mJ
P_D	Power Dissipation ^B	$T_A = 25^\circ C$	1.9
		$T_A = 70^\circ C$	1.2
T_J	Operation Junction Temperature	-55/150	$^\circ C$
T_{STG}	Storage Temperature Range	-55/150	$^\circ C$

THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^B	$t \leq 10s$	65	$^\circ C/W$
	Thermal Resistance Junction to Ambient ^{BC}			
$R_{\theta JC}$	Thermal Resistance Junction to Case	Steady-State	38	

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

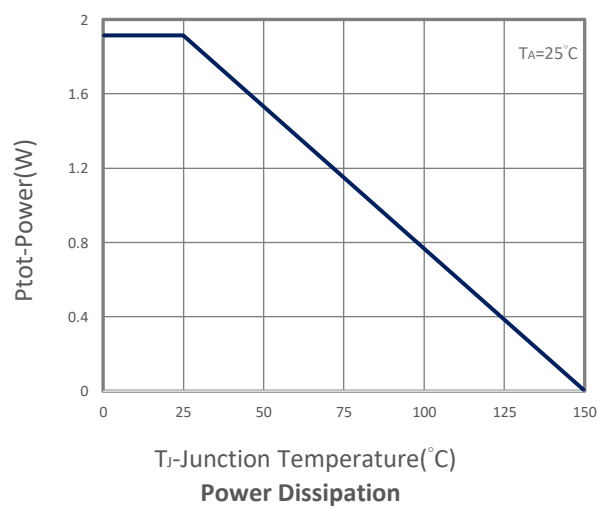
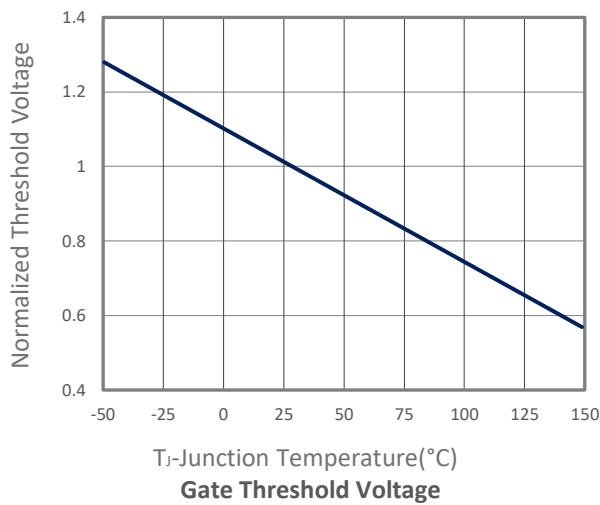
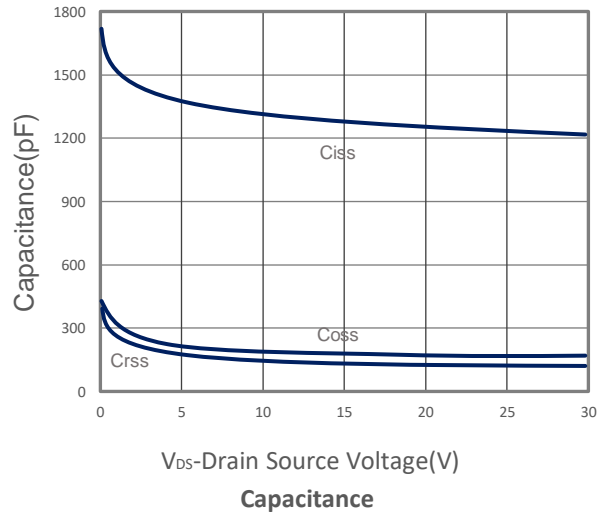
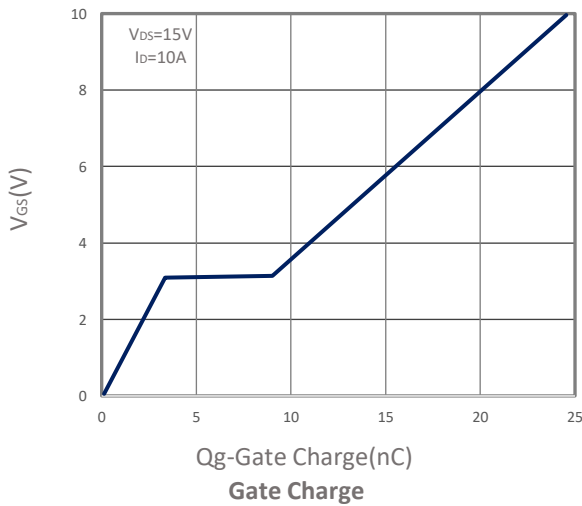
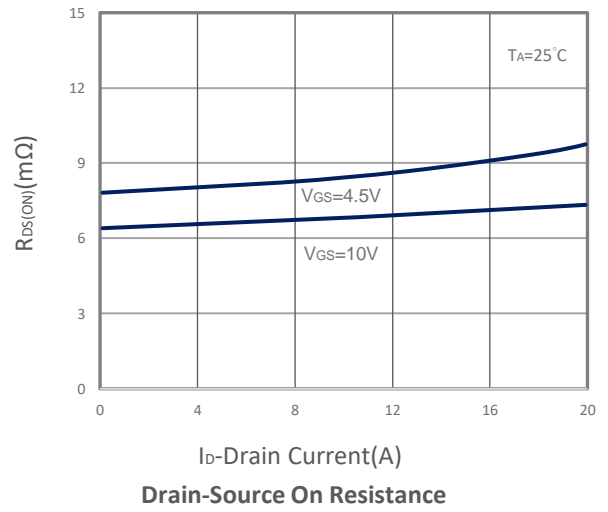
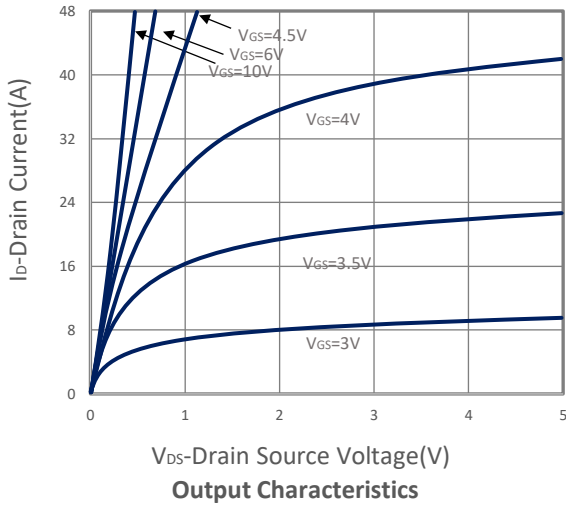
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.6	2.5	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30V, V_{GS}=0V, T_J=25^\circ\text{C}$			1	μA
		$V_{DS}=24V, V_{GS}=0V, T_J=75^\circ\text{C}$			10	
$R_{DS(ON)}$	Drain-source On-Resistance ^E	$V_{GS}=10V, I_D=12A$ $V_{GS}=4.5V, I_D=10A$		7 8	8.5 11	m Ω
G_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=10A$		8.8		S
Diode Characteristics						
V_{SD}	Diode Forward Voltage ^E	$I_S=1A, V_{GS}=0V$			1	V
I_S	Continuous Source Current				12	A
t_{rr}	Reverse Recovery Time	$I_S=10A, di/dt=100A/\mu s$		12		ns
Q_{rr}	Reverse Recovery Charge			3.5		nC
Dynamic and Switching Parameters						
Q_g	Total Gate Charge	$V_{DS}=15V, V_{GS}=10V, I_D=10A$		24.6	33.4	nC
Q_g	Total Gate Charge (4.5V)			12	15	
Q_{gs}	Gate-Source Charge			2.8	3.5	
Q_{gd}	Gate-Drain Charge			6	8.1	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$		1280		pF
C_{oss}	Output Capacitance			196		
C_{rss}	Reverse Transfer Capacitance			162		
R_g	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1\text{MHz}$		2.2		
$t_{d(on)}$	Turn-On Time	$V_{DD}=15V, V_{GEN}=10V$ $R_G=3.3\Omega, I_D=1A$		6.4	12	nS
t_r				14	27	
$t_{d(off)}$	Turn-Off Time			32.4	62	
t_f				9.2	17	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

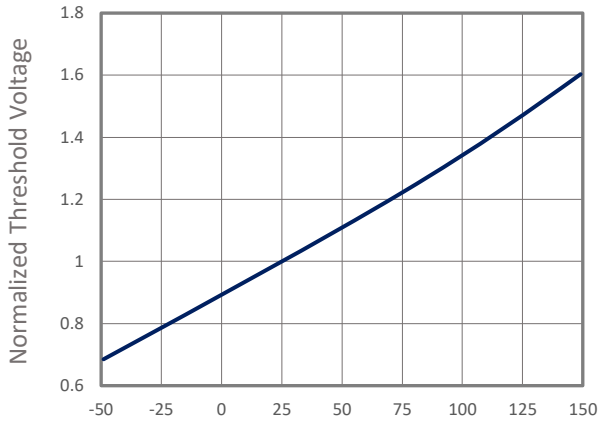
- Pulsed width limited by maximum junction temperature, $T_{J(MAX)}=150^\circ\text{C}$.
- The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board in a still air environment with maximum junction temperature $T_{J(MAX)}=150^\circ\text{C}$ (initial temperature $T_A=25^\circ\text{C}$).
- $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance ($R_{\theta JC}$) is more useful in additional heat sinking is used.
- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- The E_{AS} data shows Max, tested and pulse width limited by $T_{J(MAX)}=150^\circ\text{C}$ (initial temperature $T_J=25^\circ\text{C}$).

The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date. We assume no responsibility for any infringement of patents, patent rights, or other rights arising from the use of any information and circuitry in this datasheet.

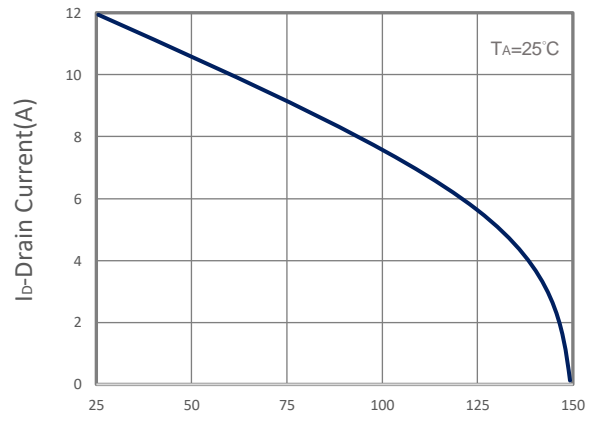
TYPICAL CHARACTERISTICS



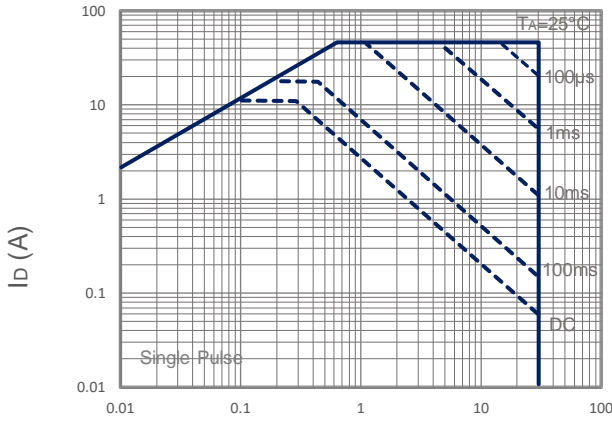
TYPICAL CHARACTERISTICS



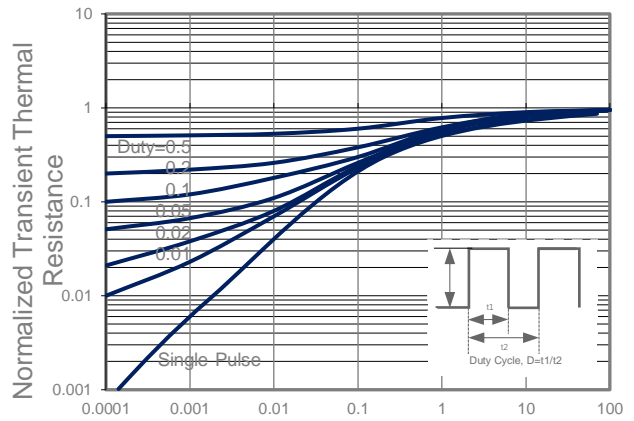
T_J-Junction Temperature(°C)
Gate Threshold Voltage



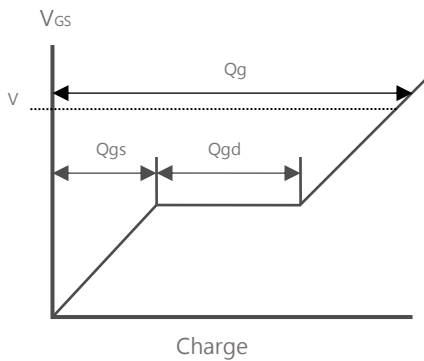
T_J-Case Temperature(°C)
Drain Current vs T_J



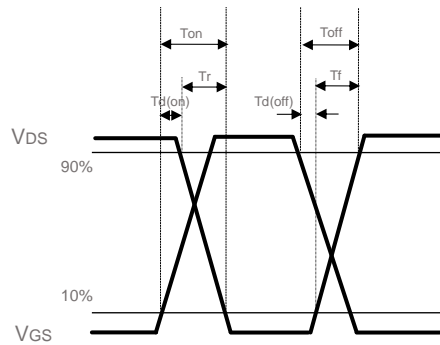
V_{DS} Voltage (V)
Maximum Safe Operation Area



Square Wave Pulse Duration(Sec)
Thermal Transient Impedance

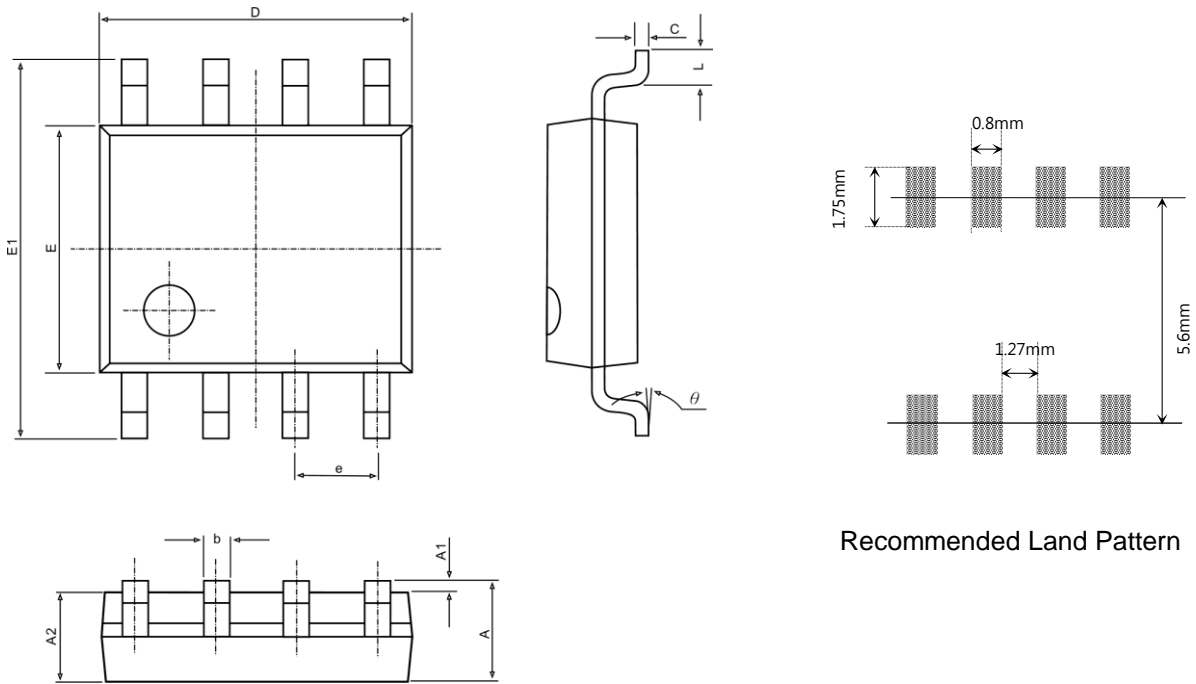


Gate Charge Waveform



Switching Time Waveform

■ SOP-8 PACKAGE DIMENSIONS



Recommended Land Pattern

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.040	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.130	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270BSC.		0.050BSC.	
L	0.400	1.270	0.016	0.005
θ	0°	8°	0°	8°