

## Single N-Channel MOSFET

### DESCRIPTION

The SMC4870NA uses trench MOSFET technology. Provides extremely low  $R_{DS(ON)}$ , Low resistance package and excellent fast switching performance. This device is ideal for efficient and fast switching applications.

### PART NUMBER INFORMATION

**SMC 4870 NA - TR G**  
 a      b      c      d      e

- a : Company name.
- b : Product Serial number.
- c : Package code      NA:DFN3.3X3.3A-8
- d : Handling code      TR:Tape&Reel
- e : Green produce code      G:RoHS Compliant

### FEATURES

**$V_{DS}=30V, I_D=35A$**

$R_{DS(ON)}=9m\Omega(Typ.)@V_{GS}=10V$   
 $R_{DS(ON)}=12m\Omega(Typ.)@V_{GS}=4.5V$

- ◆ 100% EAS Guarantee

### APPLICATIONS

- ◆ Power Management
- ◆ DC/DC Converters
- ◆ Battery Powered Systems



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_C=25^\circ C$	35
		$T_C=100^\circ C$	22
$I_{DM}$	Pulsed Drain Current <sup>B</sup>	140	A
$I_D$	Continuous Drain Current	$T_A=25^\circ C$	15
		$T_A=70^\circ C$	12
$P_D$	Power Dissipation <sup>A</sup>	$T_A=25^\circ C$	3.6
		$T_A=70^\circ C$	2.3
$I_{AS}$	Avalanche Current <sup>A</sup>	16	A
EAS	Single Pulse Avalanche energy $L=0.3mH$ <sup>B</sup>	38.4	mJ
$P_D$	Power Dissipation <sup>C</sup>	$T_C=25^\circ C$	20.8
		$T_C=100^\circ C$	8.3
$T_J$	Operation Junction Temperature	-55/150	$^\circ C$
$T_{STG}$	Storage Temperature Range	-55/150	$^\circ C$

### THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>A</sup>		35	$^\circ C/W$
	Thermal Resistance Junction to Ambient <sup>AC</sup>	$t \leq 10s$	65	
$R_{\theta JC}$	Thermal Resistance Junction to Case	Steady-State	6	

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ Unless otherwise noted)

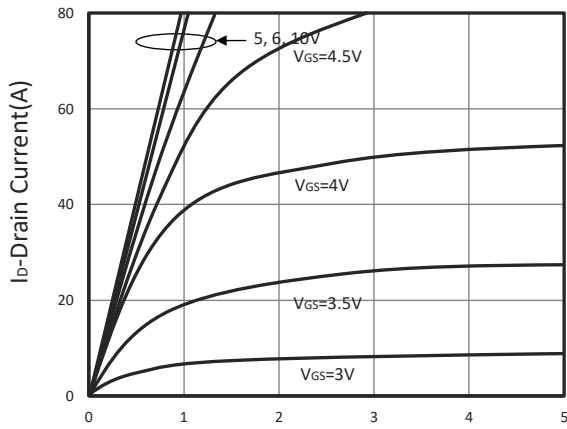
Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Static Parameters</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 $\mu$ A	30			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 $\mu$ A	1	1.6	2.5	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = $\pm$ 20V			$\pm$ 100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, T <sub>J</sub> =25 $^\circ$ C			1	$\mu$ A
		V <sub>DS</sub> =24V, V <sub>GS</sub> =0V, T <sub>J</sub> =75 $^\circ$ C			10	
R <sub>DS(ON)</sub>	Drain-source On-Resistance <sup>D</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =15A		9	11	m $\Omega$
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A		12	16	
G <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =-10A		20		S
<b>Diode Characteristics</b>						
V <sub>SD</sub>	Diode Forward Voltage <sup>E</sup>	I <sub>S</sub> =1A, V <sub>GS</sub> =0V			1	V
I <sub>S</sub>	Diode Continuous Forward Current				35	A
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =10A, di/dt=100A/ $\mu$ s		16.8		ns
Q <sub>rr</sub>	Reverse Recovery Charge			9.5		nC
<b>Dynamic and Switching Parameters<sup>E</sup></b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V, V <sub>GS</sub> =10V, I <sub>D</sub> =10A		16	22.4	nC
Q <sub>g</sub>	Total Gate Charge (4.5V)			7.9	10.9	
Q <sub>gs</sub>	Gate-Source Charge			2.6	3.6	
Q <sub>gd</sub>	Gate-Drain Charge			3.2	4.5	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz		702		pF
C <sub>oss</sub>	Output Capacitance			93		
C <sub>rss</sub>	Reverse Transfer Capacitance			68		
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, F=1MHz		2.7		$\Omega$
t <sub>d(on)</sub>	Turn-On Time	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V R <sub>G</sub> =6 $\Omega$ , I <sub>D</sub> =1A		8	15	nS
t <sub>r</sub>				10	19	
t <sub>d(off)</sub>	Turn-Off Time			22	42	
t <sub>f</sub>				6.6	13	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

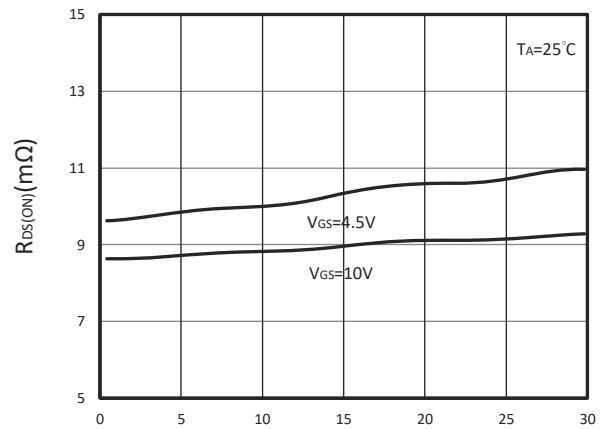
- A. Surface mounted on FR4 board using 1 in<sup>2</sup> pad size.
- B. Pulsed width limited by maximum junction temperature, T<sub>J(MAX)</sub>=150 $^\circ$ C.
- C. Using  $\leq$  10s junction-to-ambient thermal resistance is base on T<sub>J(MAX)</sub>=150 $^\circ$ C.
- D. Pulse test width  $\leq$ 300 $\mu$ s and duty cycle  $\leq$  2%.
- E. Guaranteed by design, not subject to production testing.

The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date. We assume no responsibility for any infringement of patents, patent rights, or other rights arising from the use of any information and circuitry in this datasheet.

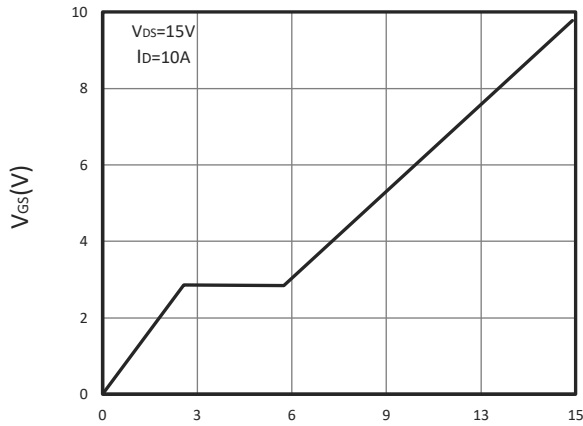
## TYPICAL CHARACTERISTICS



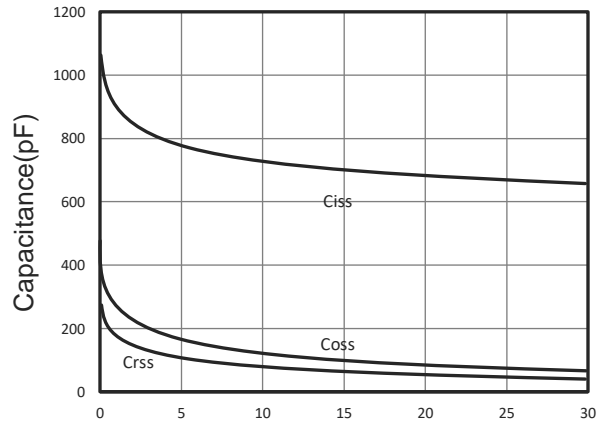
**Output Characteristics**



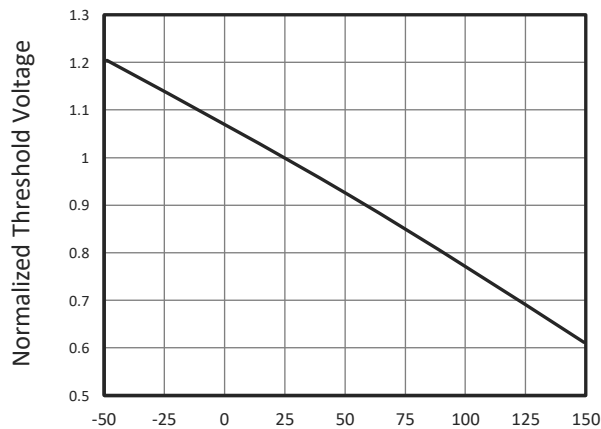
**Drain-Source On Resistance**



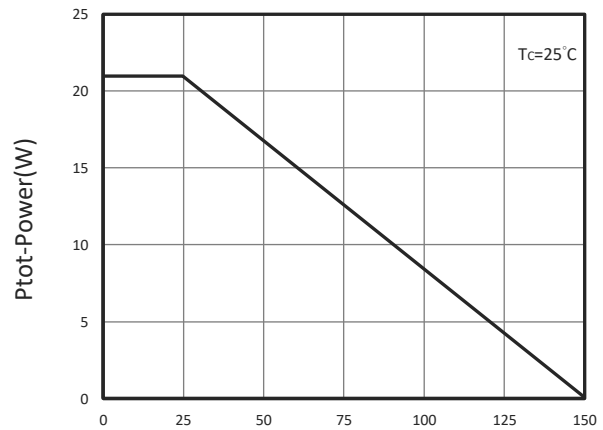
**Gate Charge**



**Capacitance**

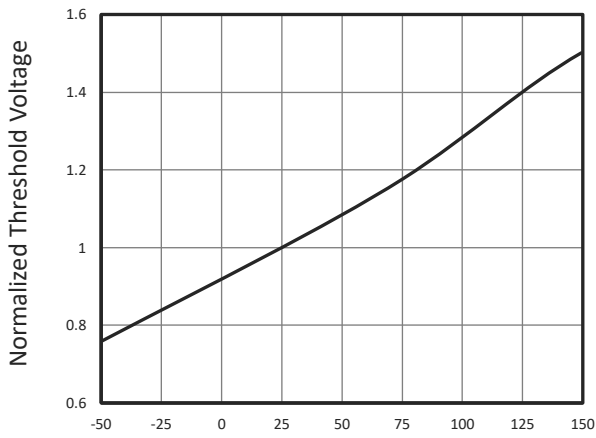


**Gate Threshold Voltage**

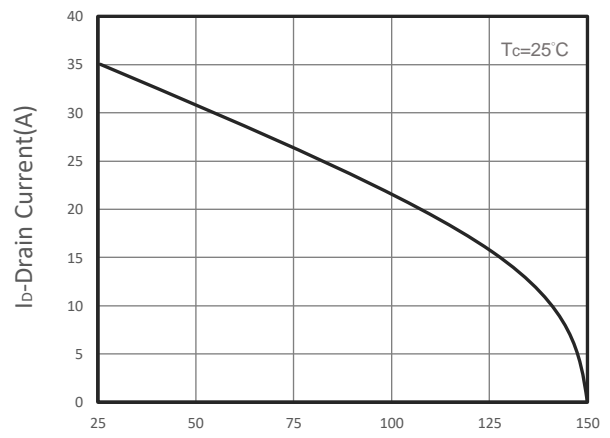


**Power Dissipation**

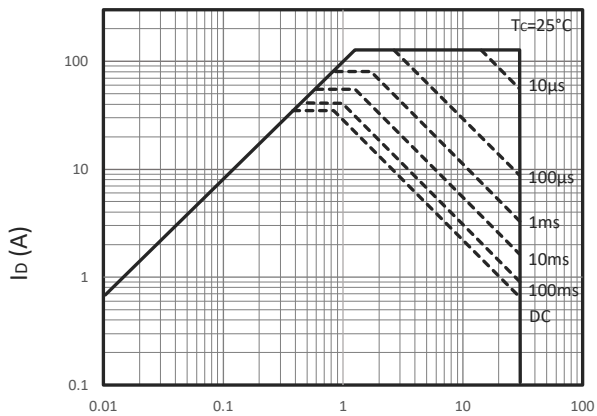
## TYPICAL CHARACTERISTICS



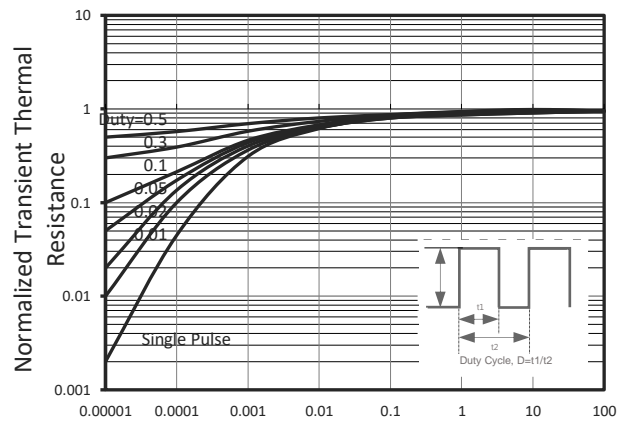
T<sub>j</sub>-Junction Temperature(°C)  
Gate Threshold Voltage



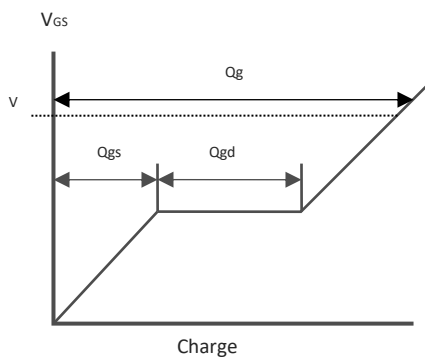
T<sub>c</sub>-Case Temperature(°C)  
Drain Current vs T<sub>c</sub>



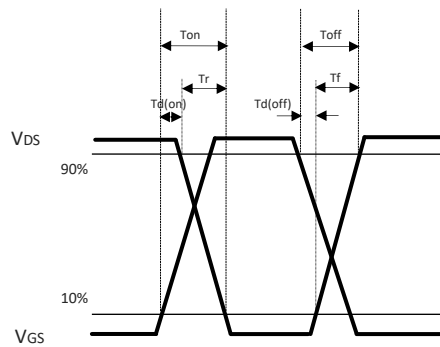
V<sub>ds</sub> Voltage (V)  
Maximum Safe Operation Area



Square Wave Pulse Duration(Sec)  
Thermal Transient Impedance

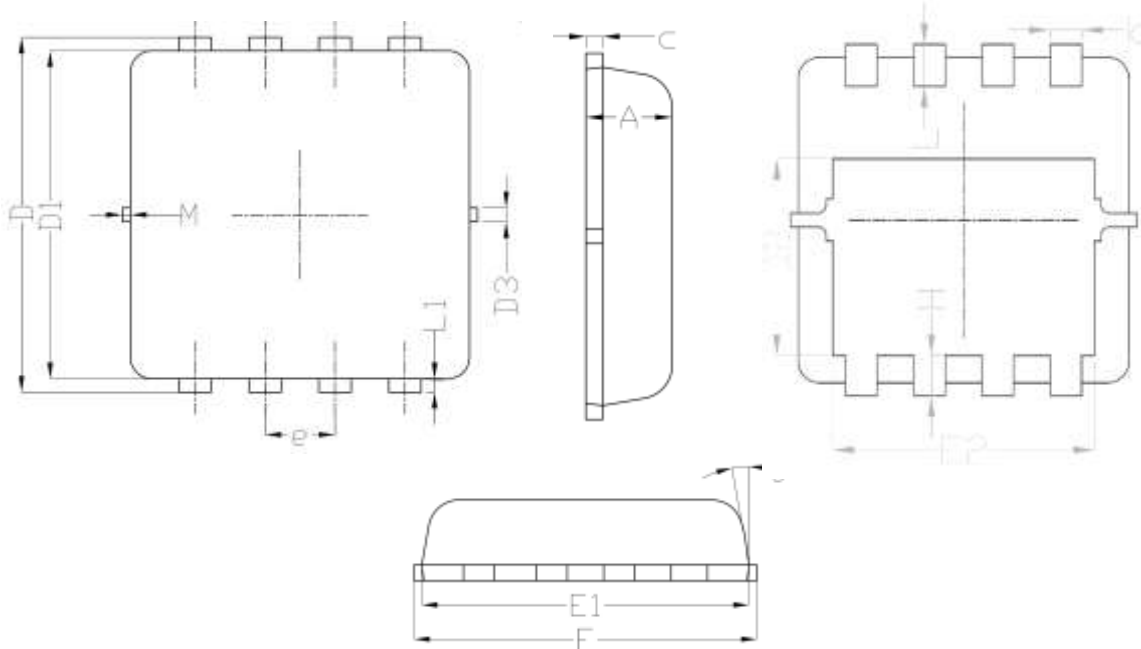


Gate Charge Waveform



Switching Time Waveform

## DFN3.3X3.3A-8 PACKAGE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
b	0.250	0.350	0.010	0.014
c	0.100	0.250	0.004	0.010
D	3.250	3.450	0.128	0.136
D1	3.000	3.200	0.118	0.126
D2	1.780	1.980	0.070	0.078
D3	-	0.130	-	0.005
E	3.200	3.400	0.126	0.134
E1	3.000	3.200	0.118	0.126
E2	2.390	2.590	0.094	0.102
e	0.65BSC.		0.026BSC.	
H	0.300	0.500	0.012	0.020
L	0.300	0.500	0.012	0.020
L1	-	0.130	-	0.005
M	-	0.150	-	0.006
Θ	0°	12°	0°	12°

Recommended Land Pattern

