SMC4863NA

Single P-Channel MOSFET

■DESCRIPTION

SMC4863NA is the P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior, fast switching performance, and withstand high energy pulse in the avalanche and commutation mode.These devices are well suited for high efficiency load switching applications.

■PART NUMBER INFORMATION

SMC 4863 NA - TR G
a b c d e

a : Company name.
b : Product Serial number.
c : Package code NA:DFN3.3X3.3A-8
d : Handling code TR:Tape&Reel
e : Green produce code G:*RoHS Compliant*

■FEATURES

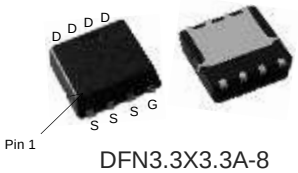
V_{DS}=-30V, I_D=-41A

$R_{DS(ON)}$=9.5mΩ(Typ.)@V_{GS}=-10V
$R_{DS(ON)}$=13mΩ(Typ.)@V_{GS}=-4.5V

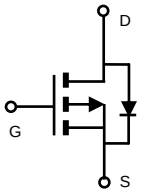
◆100% UIS and Rg tested
◆High power and current handling capability

■APPLICATIONS

◆Power Management
◆Load switch



DFN3.3X3.3A-8



■ABSOLUTE MAXIMUM RATINGS (T_A=25°C Unless otherwise noted)

Symbol	Parameter		Rating	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±25	V
I_D	Continuous Drain Current	T_C=25°C	-41	A
		T_C=100°C	-26	A
I_{DM}	Pulsed Drain Current [B]		-164	A
I_D	Continuous Drain Current	T_A=25°C	-12.8	A
		T_A=70°C	-10.3	A
P_D	Power Dissipation [A]	T_A=25°C	3.1	W
		T_A=70°C	2	W
I_{AS}	Single Pulse Avalanche Current [B]		-30	A
E_{AS}	Single Pulse Avalanche energy L=0.1mH [B]		45	mJ
P_D	Power Dissipation [C]	T_C=25°C	31.3	W
		T_C=100°C	12.5	W
T_J	Operation Junction Temperature		-55/150	°C
T_{STG}	Storage Temperature Range		-55/150	°C

■THERMAL RESISTANCE

Symbol	Parameter		Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient [A]	t≦10s		40	°C/W
	Thermal Resistance Junction to Ambient [AC]	Steady-State		60	
$R_{\theta JC}$	Thermal Resistance Junction to Case			4	

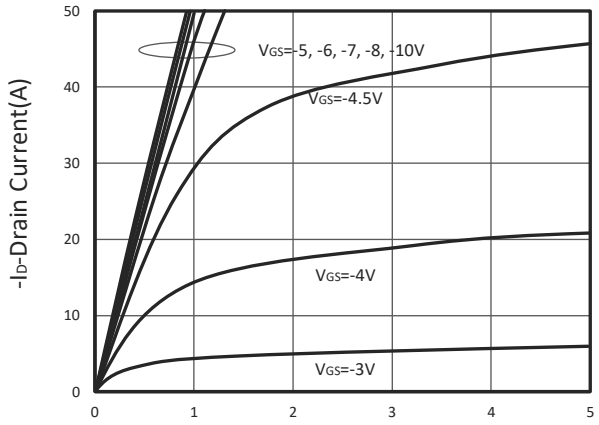
■ELECTRICAL CHARACTERISTICS(T_A=25°C Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1	-1.6	-2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V, T_J=25°C			-1	μA
		V_{DS}=-24V, V_{GS}=0V, T_J=75°C			-10	
$R_{DS(ON)}$	Drain-source On-Resistance [D]	V_{GS}=-10V, I_D=-12.8A V_{GS}=-4.5V, I_D=-10A		9.5 13	12 17	mΩ
G_{fs}	Forward Transconductance	V_{DS}=-10V, I_D=-10A		12.5		S
Diode Characteristics						
V_{SD}	Diode Forward Voltage [D]	I_S=-1A, V_{GS}=0V		-0.7	-1	V
I_S	Diode Continuous Forward Current				-41	A
t_{rr}	Reverse Recovery Time	I_S=-10A, dI/dt=100A/μs		13.8		ns
Q_{rr}	Reverse Recovery Charge			12.3		nC
Dynamic and Switching Parameters [E]						
Q_g	Total Gate Charge	V_{DS}=-15V, V_{GS}=-10V I_D=-10A		36	48.6	nC
Q_g	Total Gate Charge (4.5V)			18	24.3	
Q_{gs}	Gate-Source Charge			8.1	10.9	
Q_{gd}	Gate-Drain Charge			6.8	9.2	
C_{iss}	Input Capacitance	V_{DS}=-15V,V_{GS}=0V, f =1MHz		2150		pF
C_{oss}	Output Capacitance			298		
C_{rss}	Reverse Transfer Capacitance			135		
R_g	Gate Resistance	V_{GS}=0V, V_{DS}=0V, F=1MHz		8.8		Ω
$t_{d(on)}$	Turn-On Time	V_{DD}=-15V, V_{GEN}=-10V R_G=3.3Ω, I_D=-1A		7.7	15	nS
t_r				57.8	129	
$t_{d(off)}$	Turn-Off Time			57.5	109	
t_f				21.3	40	

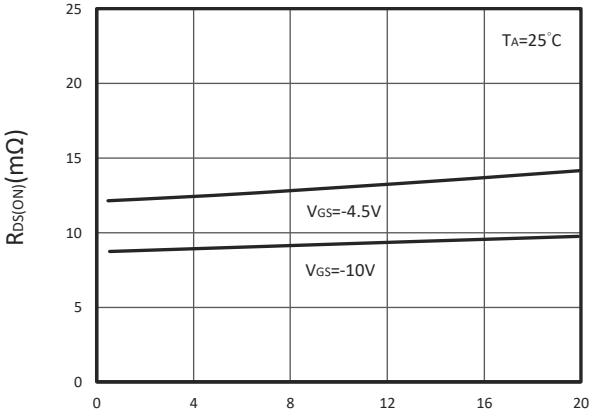
Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

A. Surface mounted on FR4 board using 1 in^2 pad size.
B. Pulsed width limited by maximum junction temperature, $T_{J(MAX)}$=150°C (initial temperature T_J=25°C).
C. Using ≤ 10s junction-to-ambient thermal resistance is base on $T_{J(MAX)}$=150°C.
D. Pulse test width ≤300μs and duty cycle ≤ 2%.
E. Guaranteed by design, not subject to production testing.

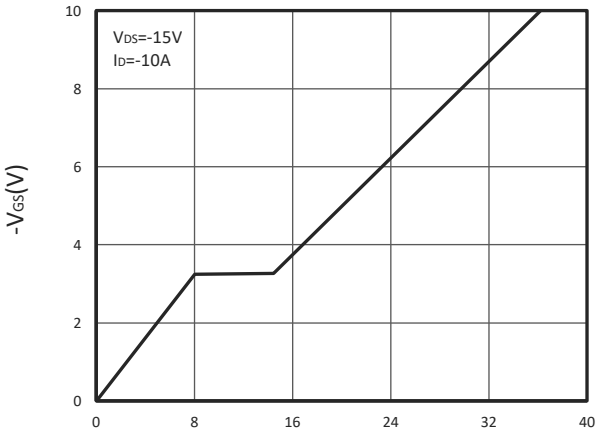
TYPICAL CHARACTERISTICS



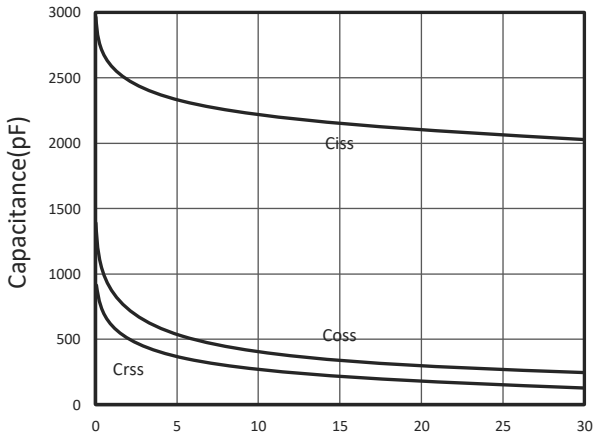
Output Characteristics



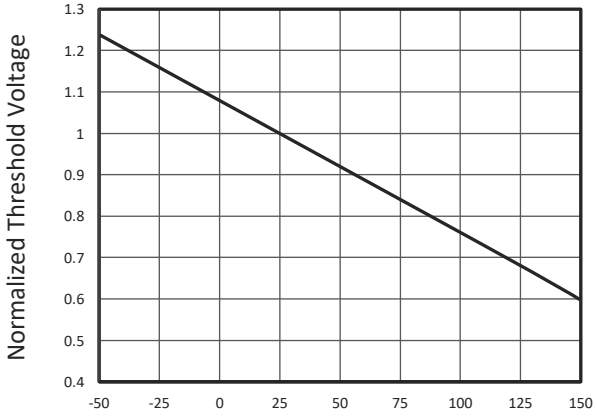
Drain-Source On Resistance



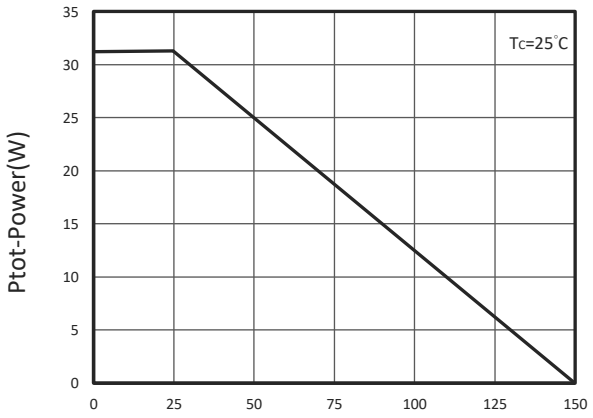
Gate Charge



Capacitance

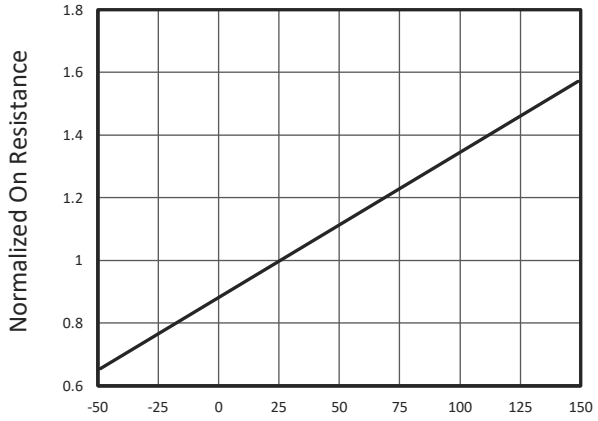


Gate Threshold Voltage



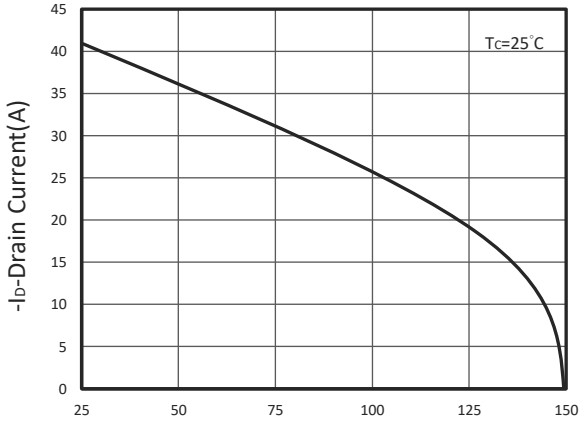
Power Dissipation

TYPICAL CHARACTERISTICS



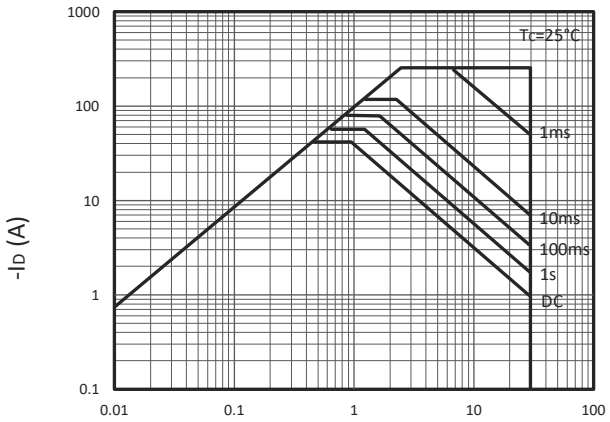
T_J-Junction Temperature(°C)

$R_{DS(ON)}$ vs Junction Temperature



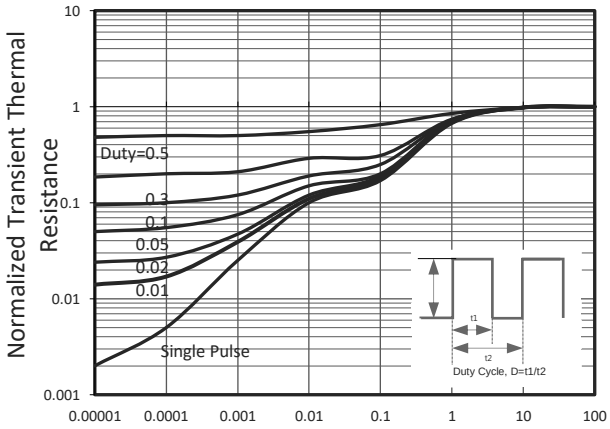
T_C-Case Temperature(°C)

Drain Current vs T_C



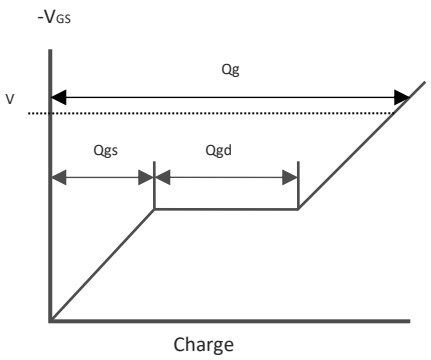
$-V_{DS}$ Voltage (V)

Maximum Safe Operation Area

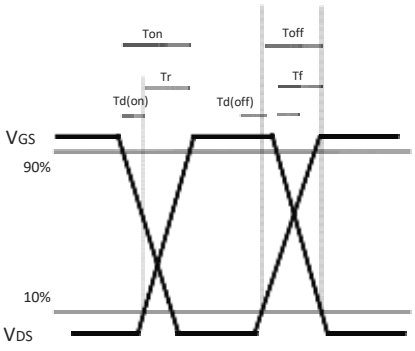


Square Wave Pulse Duration(Sec)

Thermal Transient Impedance

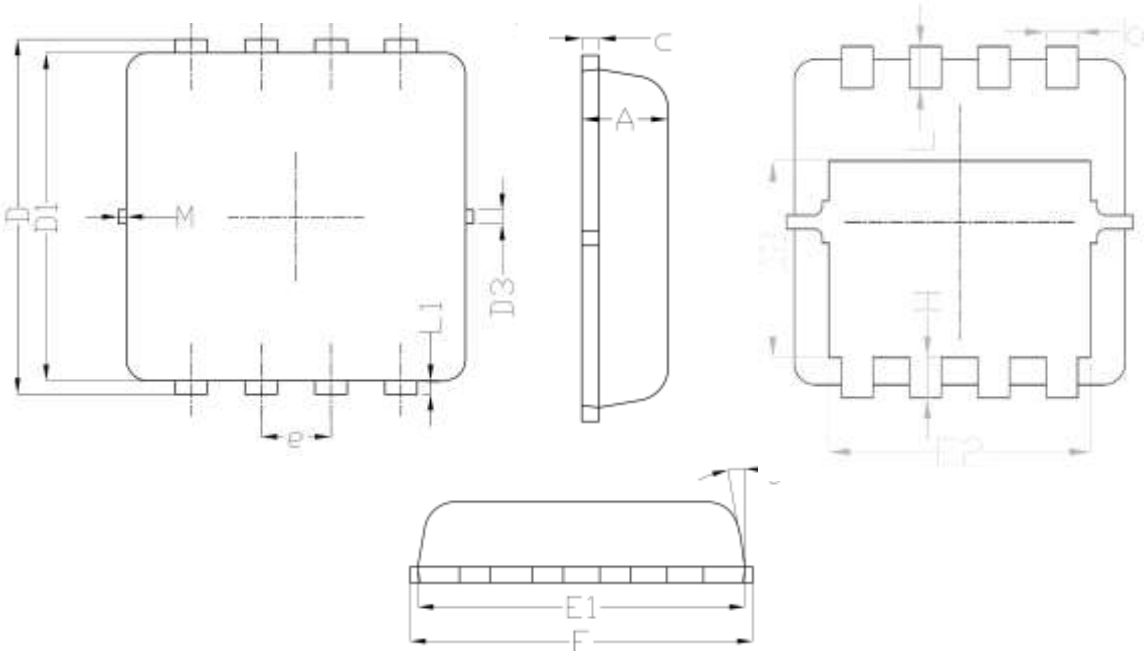


Gate Chrge Waveform



Switching Time Waveform

■DFN3.3X3.3A-8 PACKAGE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
b	0.250	0.350	0.010	0.014
c	0.100	0.250	0.004	0.010
D	3.250	3.450	0.128	0.136
D1	3.000	3.200	0.118	0.126
D2	1.780	1.980	0.070	0.078
D3	-	0.130	-	0.005
E	3.200	3.400	0.126	0.134
E1	3.000	3.200	0.118	0.126
E2	2.390	2.590	0.094	0.102
e	0.65BSC.		0.026BSC.	
H	0.300	0.500	0.012	0.020
L	0.300	0.500	0.012	0.020
L1	-	0.130	-	0.005
M	-	0.150	-	0.006
Θ	0°	12°	0°	12°

Recommended Land Pattern