

Single P-Channel MOSFET

DESCRIPTION

SMC4861 is the P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior, fast switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency load switching applications.

PART NUMBER INFORMATION

SMC 4861 NA - TR G
 a b c d e

- a : Company name.
- b : Product Serial number.
- c : Package code NA:DFN3.3X3.3A-8
- d : Handling code TR:Tape&Reel
- e : Green produce code G:RoHS Compliant

FEATURES

$V_{DS} = -30V$, $I_D = -50A$

$R_{DS(ON)} = 7m\Omega(Typ.) @ V_{GS} = -10V$
 $R_{DS(ON)} = 10m\Omega(Typ.) @ V_{GS} = -4.5V$

- ◆ 100% UIS tested
- ◆ 100% Rg tested

APPLICATIONS

- ◆ LED Application
- ◆ Power Management
- ◆ Load switch



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current *	$T_C = 25^\circ C$	-50
		$T_C = 100^\circ C$	-36.8
I_{DM}	Pulsed Drain Current ^A	-200	A
I_D	Continuous Drain Current	$T_A = 25^\circ C$	-16.5
		$T_A = 70^\circ C$	-13.2
P_D	Power Dissipation ^B	$T_A = 25^\circ C$	3.6
		$T_A = 70^\circ C$	2.3
I_{AS}	Avalanche Current ^A	-40	A
E_{AS}	Single Pulse Avalanche energy $L=0.1mH$ ^{AF}	80	mJ
P_D	Power Dissipation ^C	$T_C = 25^\circ C$	44.6
		$T_C = 100^\circ C$	18
T_J	Operation Junction Temperature	-55/150	$^\circ C$
T_{STG}	Storage Temperature Range	-55/150	$^\circ C$

THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^B	$t \leq 10s$	35	$^\circ C/W$
	Thermal Resistance Junction to Ambient ^{BD}	Steady-State	60	
$R_{\theta JC}$	Thermal Resistance Junction to Case		2.8	

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

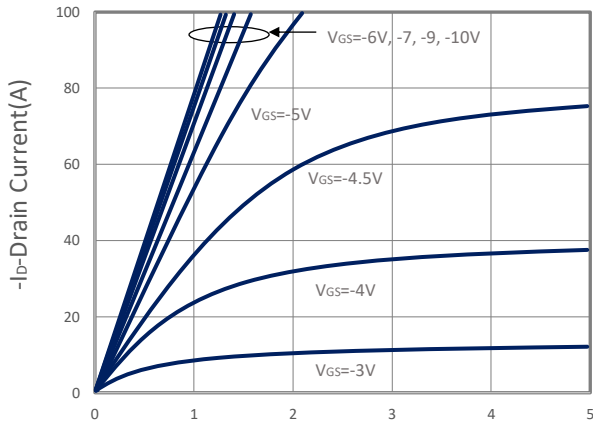
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.5	-2.5	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-30V, V_{GS}=0V, T_J=25^\circ\text{C}$			-1	μA
		$V_{DS}=-24V, V_{GS}=0V, T_J=75^\circ\text{C}$			-10	
$R_{DS(ON)}$	Drain-source On-Resistance ^E	$V_{GS}=-10V, I_D=-16.5A$ $V_{GS}=-4.5V, I_D=-10A$		7 10	8.5 13	$m\Omega$
G_{fs}	Forward Transconductance	$V_{DS}=-10V, I_D=-10A$		14.8		S
Diode Characteristics						
V_{SD}	Diode Forward Voltage ^E	$I_S=-1A, V_{GS}=0V$		-0.7	-1	V
I_S	Continuous Source Current [*]				-50	A
t_{rr}	Reverse Recovery Time	$I_S=-10A, di/dt=100A/\mu s$		21		ns
Q_{rr}	Reverse Recovery Charge			15.5		nC
Dynamic and Switching Parameters						
Q_g	Total Gate Charge (10V)	$V_{DS}=-15V, V_{GS}=-10V, I_D=-10A$		61	85	nC
Q_g	Total Gate Charge (4.5V)			30	42	
Q_{gs}	Gate-Source Charge			10.6	14.3	
Q_{gd}	Gate-Drain Charge			9	12.6	
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$		3376		pF
C_{oss}	Output Capacitance			369		
C_{rss}	Reverse Transfer Capacitance			224		
R_g	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1\text{MHz}$		8.2		Ω
$t_{d(on)}$	Turn-On Time ^E	$V_{DD}=-15V, V_{GEN}=-10V,$ $R_G=3\Omega, I_D=-1A$		24	46	nS
t_r				11.6	22	
$t_{d(off)}$	Turn-Off Time ^E			78.8	150	
t_f				33.8	63	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

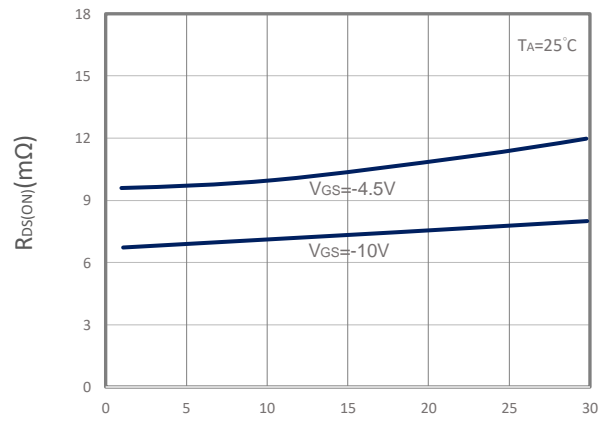
- A. Pulsed width limited by maximum junction temperature, $T_{J(MAX)}=150^\circ\text{C}$.
- B. Measure the value in a still air environment at $T_A=25^\circ\text{C}$, using an installation mounted on a 1 in2 FR-4 board, maximum junction temperature $T_{J(MAX)}=150^\circ\text{C}$.
- C. Using junction-to-case thermal resistance, dissipation limit in the case of additional heat.
- D. $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance ($R_{\theta JC}$) is more useful in additional heat sinking is used.
- E. The pulse test width is $\leq 300\mu s$ and the duty cycle $\leq 2\%$.
- F. The EAS data shows Maximum, tested and pulse width limited by maximum.
- *. The maximum rating current is limited by wire bonding.

The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date. We assume no responsibility for any infringement of patents, patent rights, or other rights arising from the use of any information and circuitry in this datasheet.

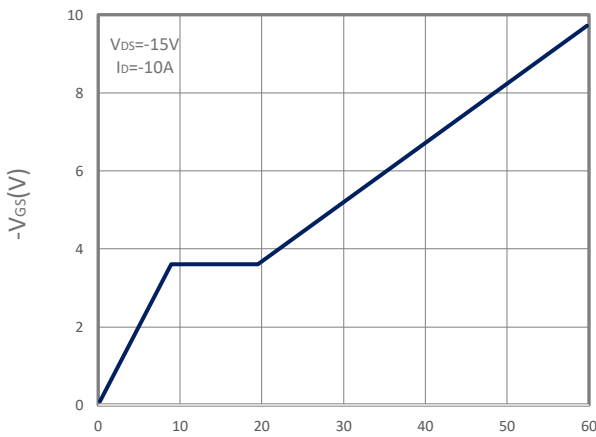
TYPICAL CHARACTERISTICS



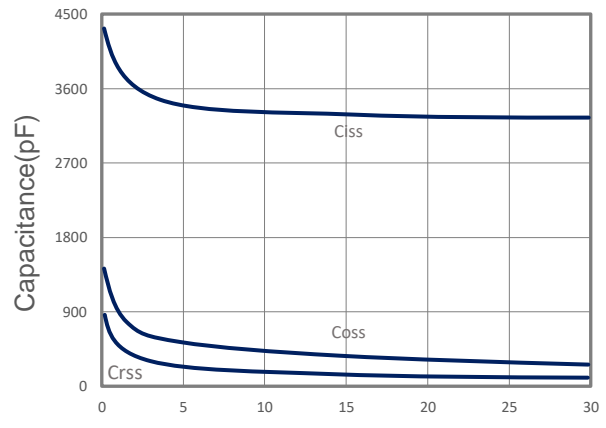
Output Characteristics



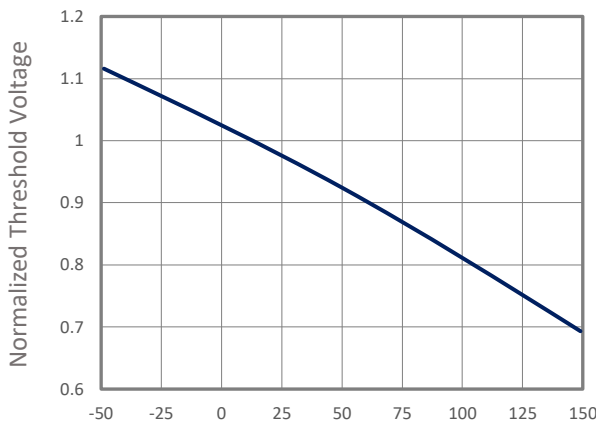
Drain-Source On Resistance



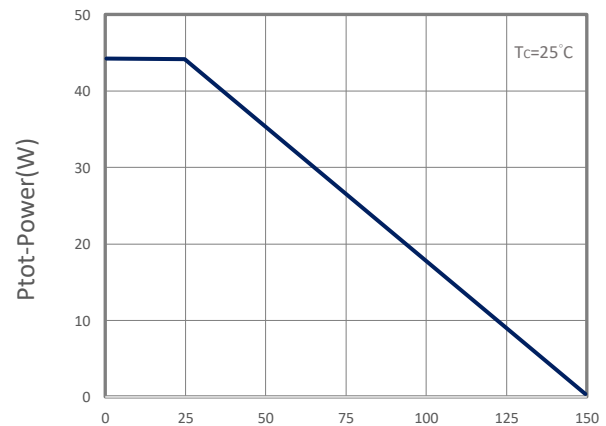
Gate Charge



Capacitance

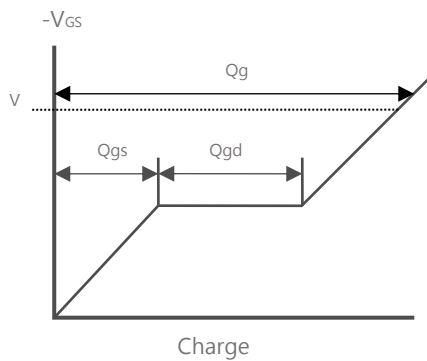
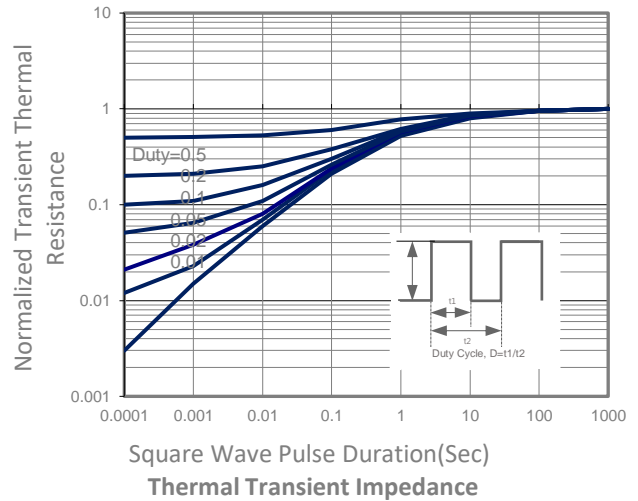
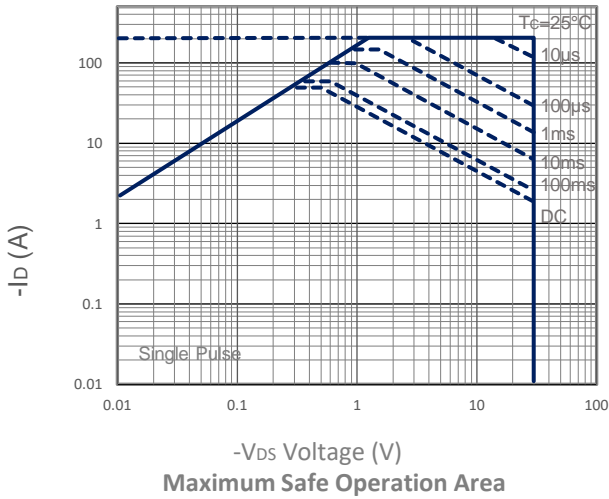
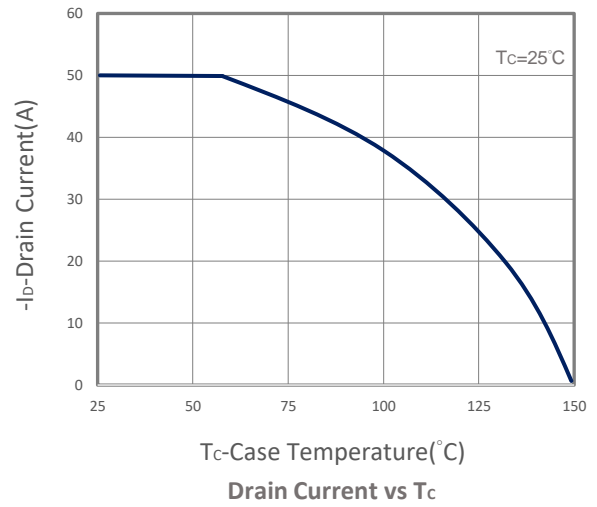
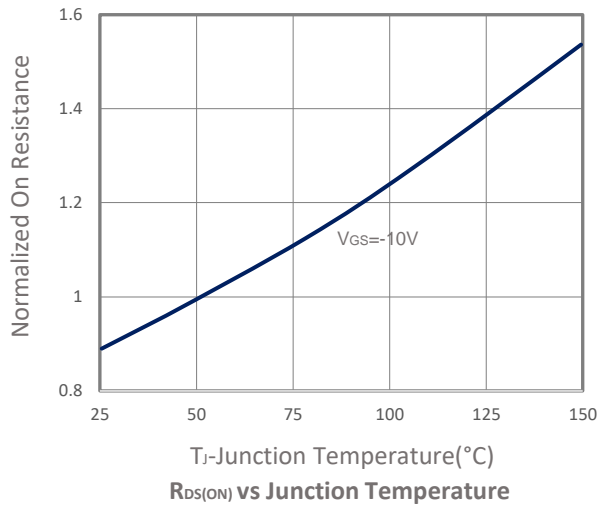


Gate Threshold Voltage

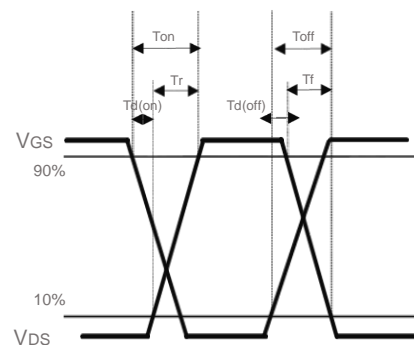


Power Dissipation

TYPICAL CHARACTERISTICS

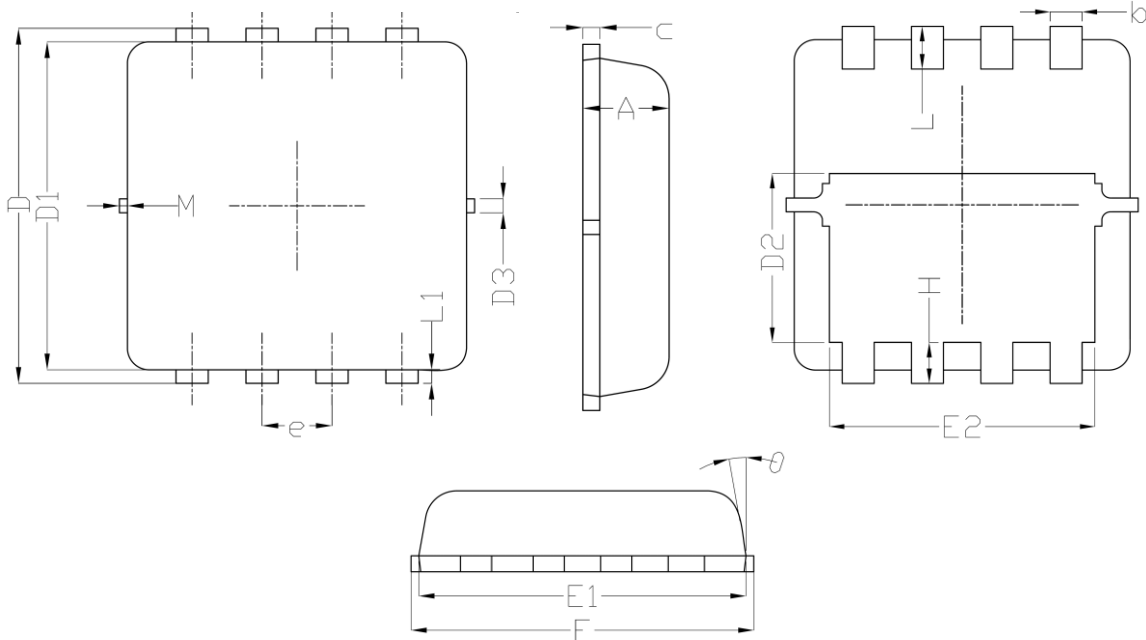


Gate Charge Waveform



Switching Time Waveform

DFN3.3X3.3A-8 PACKAGE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
b	0.250	0.350	0.010	0.014
c	0.100	0.250	0.004	0.010
D	3.300	3.400	0.130	0.134
D1	3.250	3.450	0.128	0.136
D2	1.780	1.980	0.070	0.078
D3	-	0.130	-	0.005
E	3.200	3.400	0.126	0.134
E1	3.000	3.200	0.118	0.126
E2	2.390	2.590	0.094	0.102
e	0.65BSC.		0.026BSC.	
H	0.300	0.500	0.012	0.020
L	0.300	0.500	0.012	0.020
L1	-	0.130	-	0.005
M	-	0.150	-	0.006
θ	0°	12°	0°	15°

Recommended Land Pattern

