

Single N-Channel MOSFET

DESCRIPTION

SMC4860NA is the N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior, fast switching performance. These devices are well suited for high efficiency fast switching applications.

PART NUMBER INFORMATION

SMC 4860 NA - TR G
 a b c d e

a : Company name.
 b : Product Serial number.
 c : Package code NA:DFN3.3X3.3A-8
 d : Handling code TR:Tape&Reel
 e : Green produce code G:RoHS Compliant

FEATURES

$V_{DS}=30V, I_D=70A$

$R_{DS(ON)}=3.3m\Omega(Typ.)@V_{GS}=10V$

$R_{DS(ON)}=4.3m\Omega(Typ.)@V_{GS}=4.5V$

- ◆ 100% EAS Guaranteed
- ◆ Very Low $R_{DS(ON)}$
- ◆ High power and current handling capability

APPLICATIONS

- ◆ Power Management
- ◆ Battery Powered Systems.
- ◆ DC/DC Converters



ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}C$ Unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current *	$T_C=25^{\circ}C$	70
		$T_C=100^{\circ}C$	44.2
I_{DM}	Pulsed Drain Current ^B	140	A
I_D	Continuous Drain Current ($V_{GS}=10V$)	$T_A=25^{\circ}C$	23
		$T_A=70^{\circ}C$	18.3
P_D	Power Dissipation ^A	$T_A=25^{\circ}C$	3.6
		$T_A=70^{\circ}C$	2.3
I_{AS}	Avalanche Current ^A	30	A
EAS	Single Pulse Avalanche energy $L=0.1mH$ ^B	45	mJ
P_D	Power Dissipation ^C	$T_C=25^{\circ}C$	33
		$T_C=100^{\circ}C$	13.2
T_J	Operation Junction Temperature	-55/150	$^{\circ}C$
T_{STG}	Storage Temperature Range	-55/150	$^{\circ}C$

THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^A	$t \leq 10s$	35	$^{\circ}C/W$
	Thermal Resistance Junction to Ambient ^{AC}			
$R_{\theta JC}$	Thermal Resistance Junction to Case	Steady-State	3.8	

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ Unless otherwise noted)

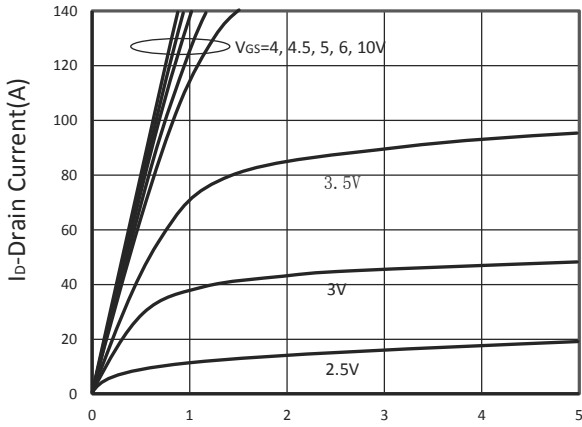
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μ A	1.2	1.6	2.5	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} = \pm 20V			\pm 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V, T _J =25 $^\circ$ C			1	μ A
		V _{DS} =24V, V _{GS} =0V, T _J =75 $^\circ$ C			10	
R _{DS(ON)}	Drain-source On-Resistance ^D	V _{GS} =10V, I _D =20A V _{GS} =4.5V, I _D =15A		3.3 4.3	4.2 5.6	m Ω
G _{fs}	Forward Transconductance	V _{DS} =10V, I _D =10A		30		S
Diode Characteristics						
V _{SD}	Diode Forward Voltage ^D	I _S =1A, V _{GS} =0V			1	V
I _S	Diode Continuous Forward Current [*]				50	A
t _{rr}	Reverse Recovery Time	I _S =20A, dI/dt=100A/ μ s		34		ns
Q _{rr}	Reverse Recovery Charge			25		nC
Dynamic and Switching Parameters^E						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _D =20A		62.4	87.4	nC
Q _g	Total Gate Charge (4.5V)			30.6	42.8	
Q _{gs}	Gate-Source Charge			5	7	
Q _{gd}	Gate-Drain Charge			13	18.2	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		2950		pF
C _{oss}	Output Capacitance			390		
C _{rss}	Reverse Transfer Capacitance			285		
R _g	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz		2		Ω
t _{d(on)}	Turn-On Time	V _{DD} =15V, V _{GEN} =10V R _G =3 Ω , I _D =10A		12	22	nS
t _r				16	30	
t _{d(off)}	Turn-Off Time			27	51	
t _f				11	21	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

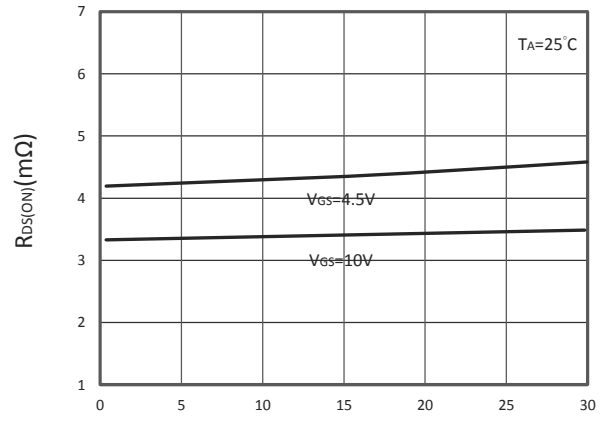
- A. Surface mounted on FR4 board using 1 in² pad size.
- B. Pulsed width limited by maximum junction temperature, T_{J(MAX)}=150 $^\circ$ C(initial temperature T_J=25 $^\circ$ C).
- C. Using \leq 10s junction-to-ambient thermal resistance is base on T_{J(MAX)}=150 $^\circ$ C.
- D. Pulse test width \leq 300 μ s and duty cycle \leq 2%.
- E. Guaranteed by design, not subject to production testing.
- *. The maximum rating current is limited by bonding wire.

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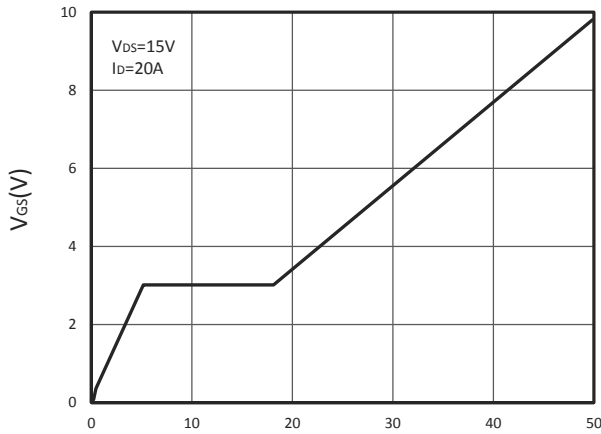
TYPICAL CHARACTERISTICS



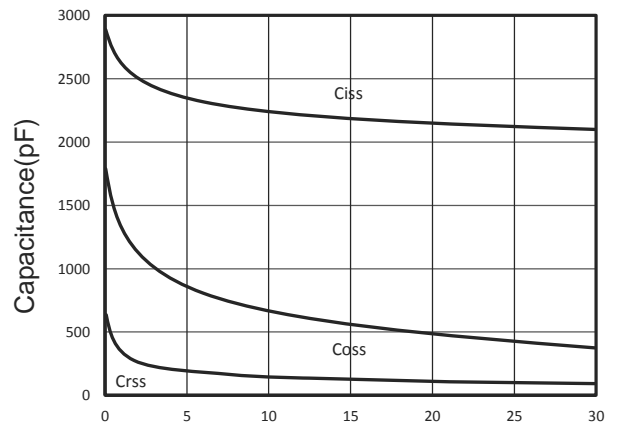
Output Characteristics



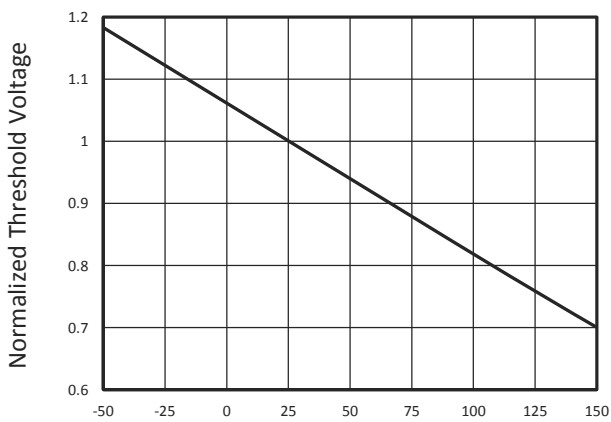
Drain-Source On Resistance



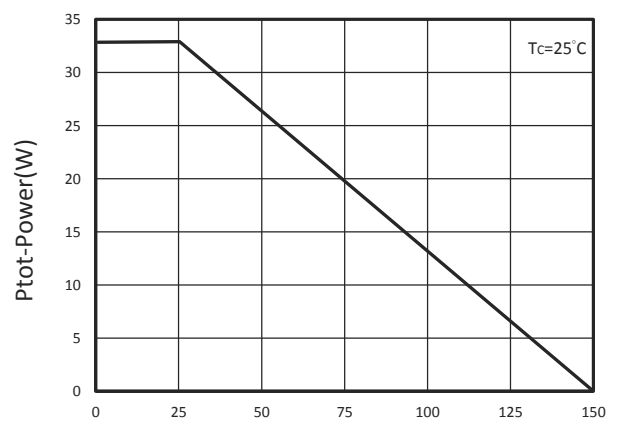
Gate Charge



Capacitance

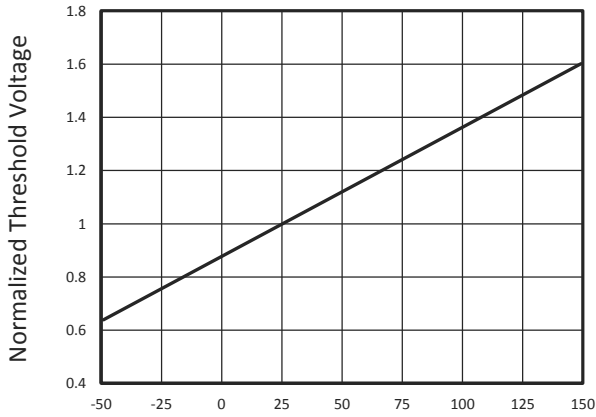


Gate Threshold Voltage

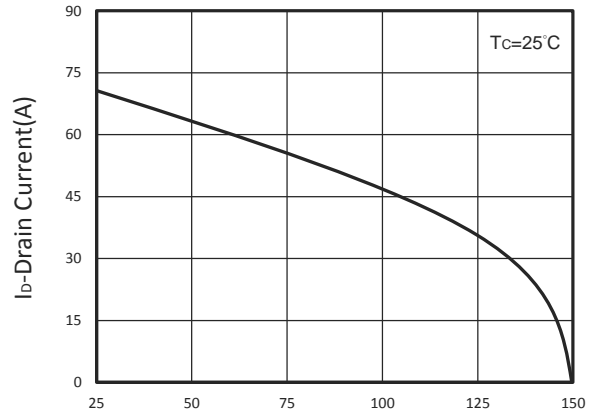


Power Dissipation

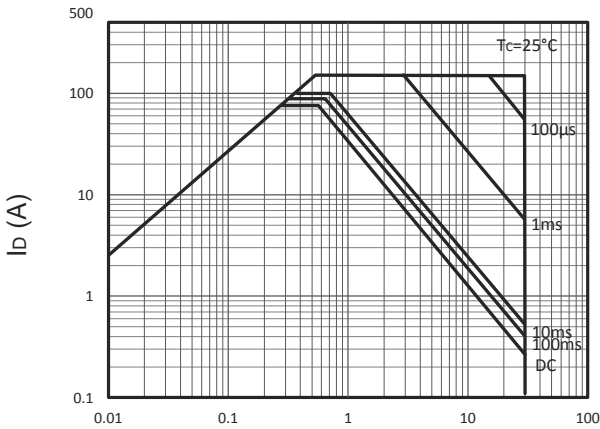
TYPICAL CHARACTERISTICS



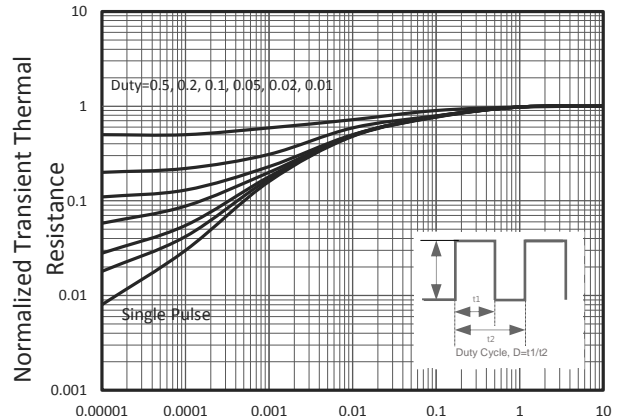
T_J-Junction Temperature(°C)
Gate Threshold Voltage



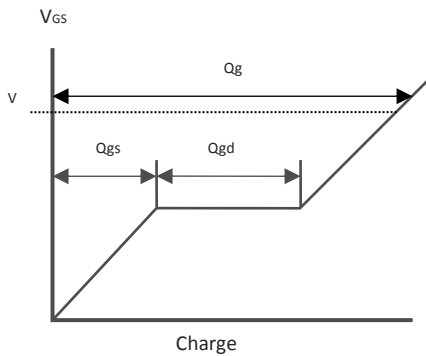
T_C-Case Temperature(°C)
Drain Current vs T_C



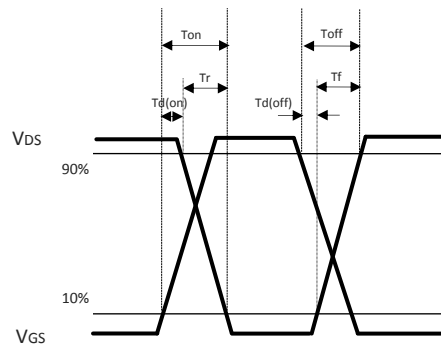
V_{DS} Voltage (V)
Maximum Safe Operation Area



Square Wave Pulse Duration(Sec)
Thermal Transient Impedance

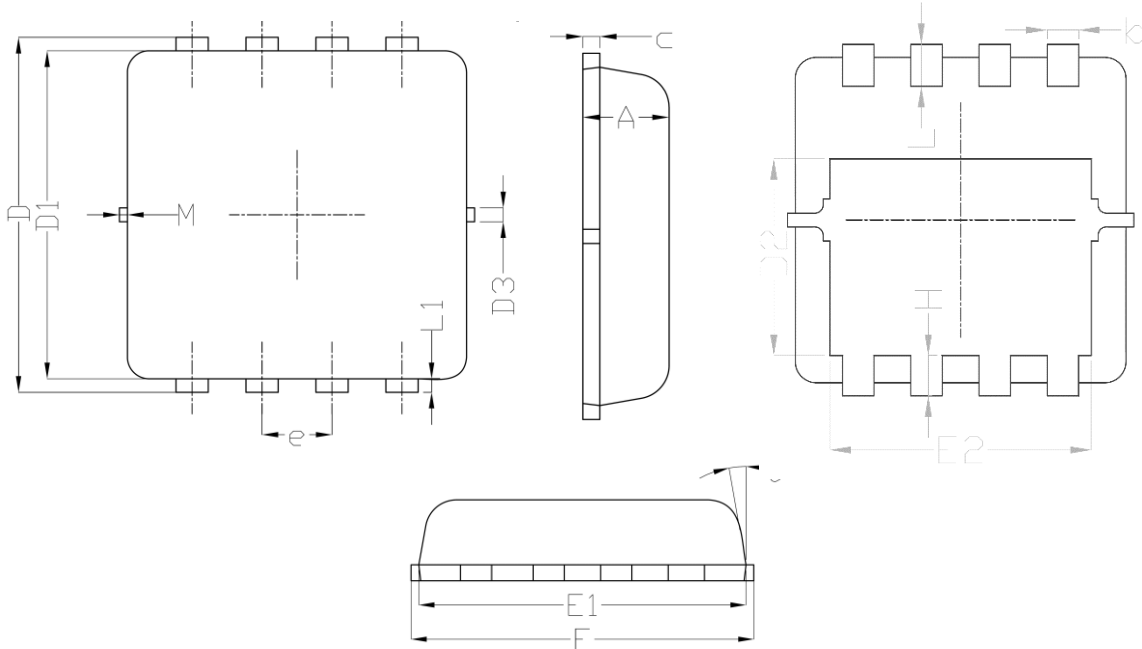


Gate Chrg Waveform



Switching Time Waveform

DFN3.3X3.3A-8 PACKAGE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
b	0.250	0.350	0.010	0.014
c	0.100	0.250	0.004	0.010
D	3.250	3.450	0.128	0.136
D1	3.000	3.200	0.118	0.126
D2	1.780	1.980	0.070	0.078
D3	-	0.130	-	0.005
E	3.200	3.400	0.126	0.134
E1	3.000	3.200	0.118	0.126
E2	2.390	2.590	0.094	0.102
e	0.65BSC.		0.026BSC.	
H	0.300	0.500	0.012	0.020
L	0.300	0.500	0.012	0.020
L1	-	0.130	-	0.005
M	-	0.150	-	0.006
Θ	0°	12°	0°	12°

Recommended Land Pattern

