

## Single N-Channel MOSFET

### DESCRIPTION

SMC4618NA is the N-Channel enhancement mode power field effect transistors are using trench technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior fast switching performance, and withstand high energy pulse in the avalanche and commutation mode.

### PART NUMBER INFORMATION

#### SMC 4618 NA - TR G

a b c d e

- a : Company name.
- b : Product Serial number.
- c : Package code      NA:DFN3.3X3.3A-8
- d : Handling code      TR:Tape&Reel
- e : Green produce code    G:RoHS Compliant

### FEATURES

**$V_{DS}=60V, I_D=30A$**

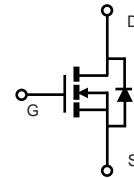
$R_{DS(ON)}=15m\Omega(Typ.)@V_{GS}=10V$

$R_{DS(ON)}=18m\Omega(Typ.)@V_{GS}=4.5V$

- ◆ 100% EAS and Guaranteed
- ◆ Improved dv/dt capability
- ◆ High power and current handling capability

### APPLICATIONS

- ◆ SMPS Synchronous Rectification
- ◆ LED Application
- ◆ Power Management
- ◆ Motor Drive



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DSS}$	Drain-Source Voltage	60	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_C=25^\circ C$	30
		$T_C=100^\circ C$	19
$I_{DM}$	Pulsed Drain Current <sup>B</sup>	120	A
$I_D$	Continuous Drain Current	$T_A=25^\circ C$	11
		$T_A=70^\circ C$	8.8
$P_D$	Power Dissipation <sup>A</sup>	$T_A=25^\circ C$	4.2
		$T_A=70^\circ C$	2.7
$I_{AS}$	Avalanche Current <sup>B</sup>	30	A
EAS	Single Pulse Avalanche energy $L=0.1mH$ <sup>B</sup>	45	mJ
$P_D$	Power Dissipation <sup>C</sup>	$T_C=25^\circ C$	31
		$T_C=100^\circ C$	12.5
$T_J$	Operation Junction Temperature	-55/150	$^\circ C$
$T_{STG}$	Storage Temperature Range	-55/150	$^\circ C$

### THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>A</sup>	$t \leq 10s$	30	$^\circ C/W$
	Thermal Resistance Junction to Ambient <sup>AC</sup>	Steady-State	60	
$R_{\theta JC}$	Thermal Resistance Junction to Case		4	

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ Unless otherwise noted)

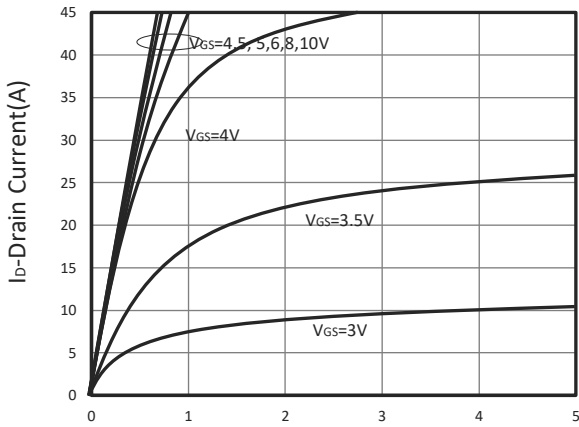
Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Static Parameters</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.8	2.5	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C			1	μA
		V <sub>DS</sub> =48V, V <sub>GS</sub> =0V, T <sub>J</sub> =75°C			10	
R <sub>DS(ON)</sub>	Drain-source On-Resistance <sup>D</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =11A V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A		15 18	18 23	mΩ
G <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =10A		9		S
<b>Diode Characteristics</b>						
V <sub>SD</sub>	Diode Forward Voltage <sup>D</sup>	I <sub>S</sub> =1A, V <sub>GS</sub> =0V			1	V
I <sub>S</sub>	Diode Continuous Forward Current				15.1	A
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =10A, dI/dt=100A/μs		22		ns
Q <sub>rr</sub>	Reverse Recovery Charge			18		nC
<b>Dynamic and Switching Parameters<sup>E</sup></b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =30V, V <sub>GS</sub> =10V, I <sub>D</sub> =10A		25.2	34	nC
Q <sub>g</sub>	Total Gate Charge (4.5V)			12	16.2	
Q <sub>gs</sub>	Gate-Source Charge			5	6.8	
Q <sub>gd</sub>	Gate-Drain Charge			5.8	8.1	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1MHz		1620		pF
C <sub>oss</sub>	Output Capacitance			125		
C <sub>rss</sub>	Reverse Transfer Capacitance			70		
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, F=1MHz		2.2		Ω
t <sub>d(on)</sub>	Turn-On Time	V <sub>DD</sub> =30V, V <sub>GS</sub> =10V R <sub>G</sub> =6Ω, I <sub>D</sub> =1A		15	29	nS
t <sub>r</sub>				8.2	16	
t <sub>d(off)</sub>	Turn-Off Time			32	61	
T <sub>f</sub>				10	19	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

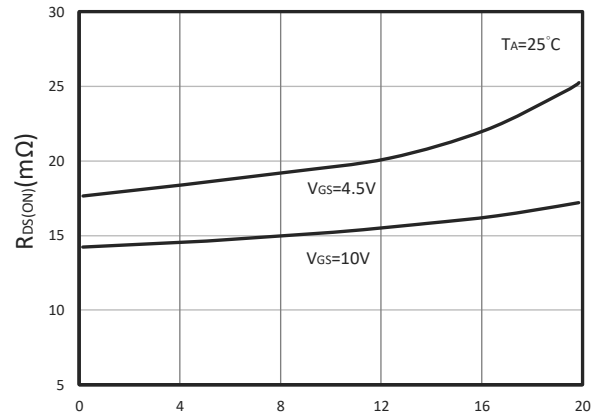
- A. Surface mounted on FR4 board using 1 in<sup>2</sup> pad size.
- B. Pulsed width limited by maximum junction temperature, T<sub>J(MAX)</sub>=150°C.
- C. Using ≤ 10s junction-to-ambient thermal resistance is base on T<sub>J(MAX)</sub>=150°C.
- D. Pulse test width ≤ 300μs and duty cycle ≤ 2%.
- E. Guaranteed by design, not subject to production testing.

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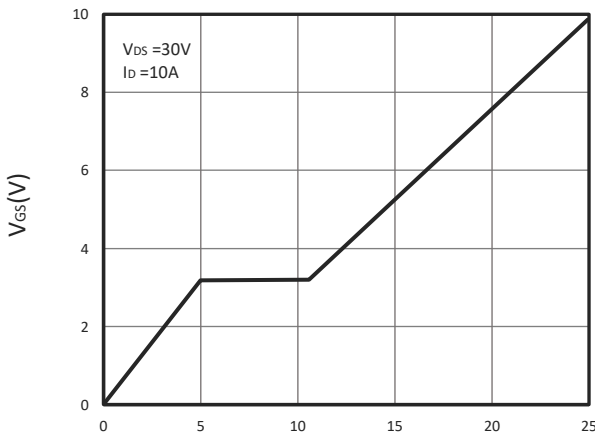
## TYPICAL CHARACTERISTICS



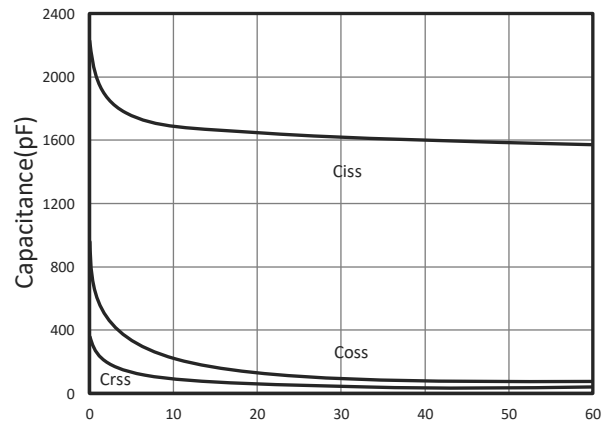
V<sub>DS</sub>-Drain Source Voltage(V)  
Output Characteristics



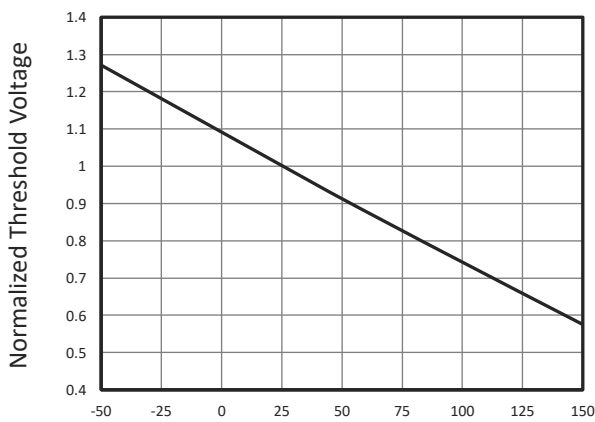
Id-Drain Current(A)  
Drain-Source On Resistance



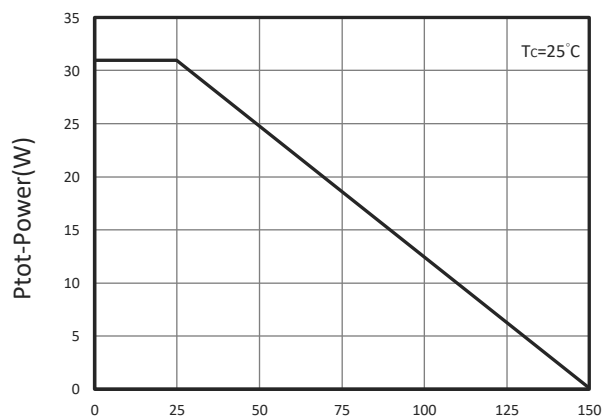
Q<sub>g</sub>-Gate Charge(nC)  
Gate Charge



V<sub>DS</sub>-Drain Source Voltage(V)  
Capacitance

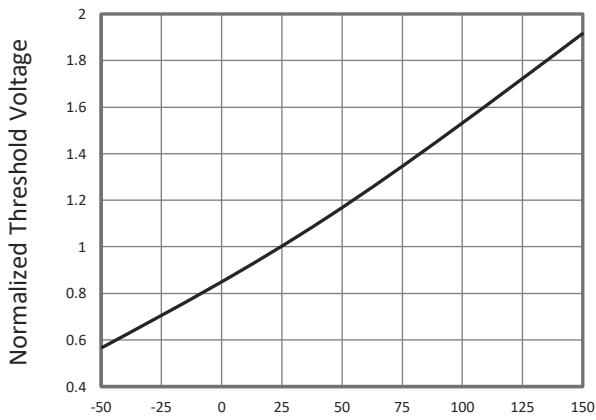


T<sub>J</sub>-Junction Temperature(°C)  
Gate Threshold Voltage

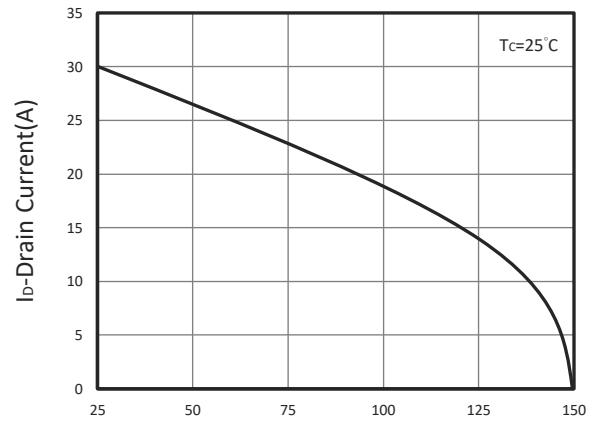


T<sub>C</sub>-Case Temperature(°C)  
Power Dissipation

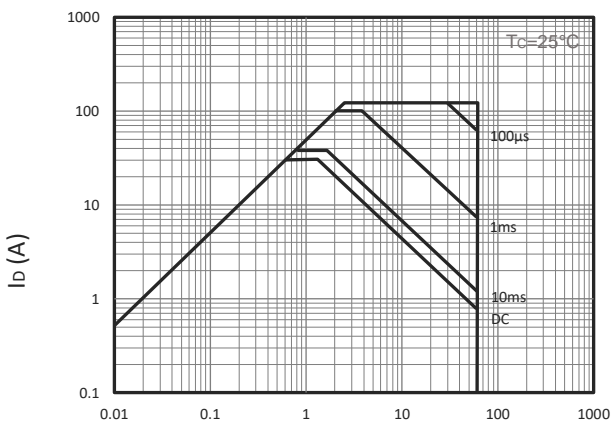
## TYPICAL CHARACTERISTICS



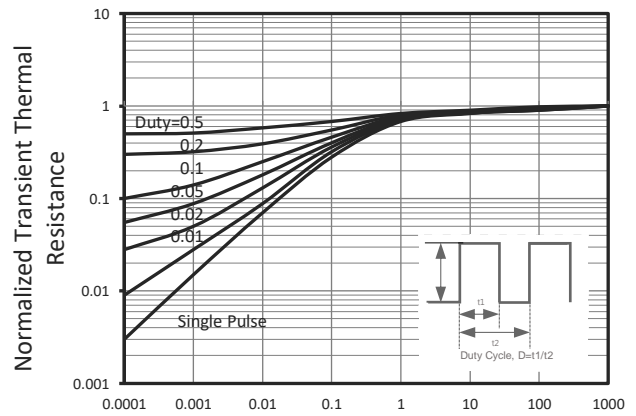
T<sub>j</sub>-Junction Temperature(°C)  
Gate Threshold Voltage



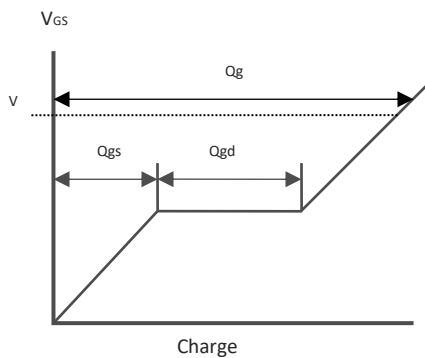
T<sub>c</sub>-cSAE Temperature(°C)  
Drain Current vs T<sub>c</sub>



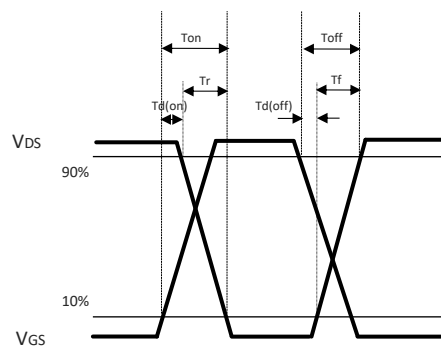
V<sub>ds</sub> Voltage (V)  
Maximum Safe Operation Area



Square Wave Pulse Duration(Sec)  
Thermal Transient Impedance

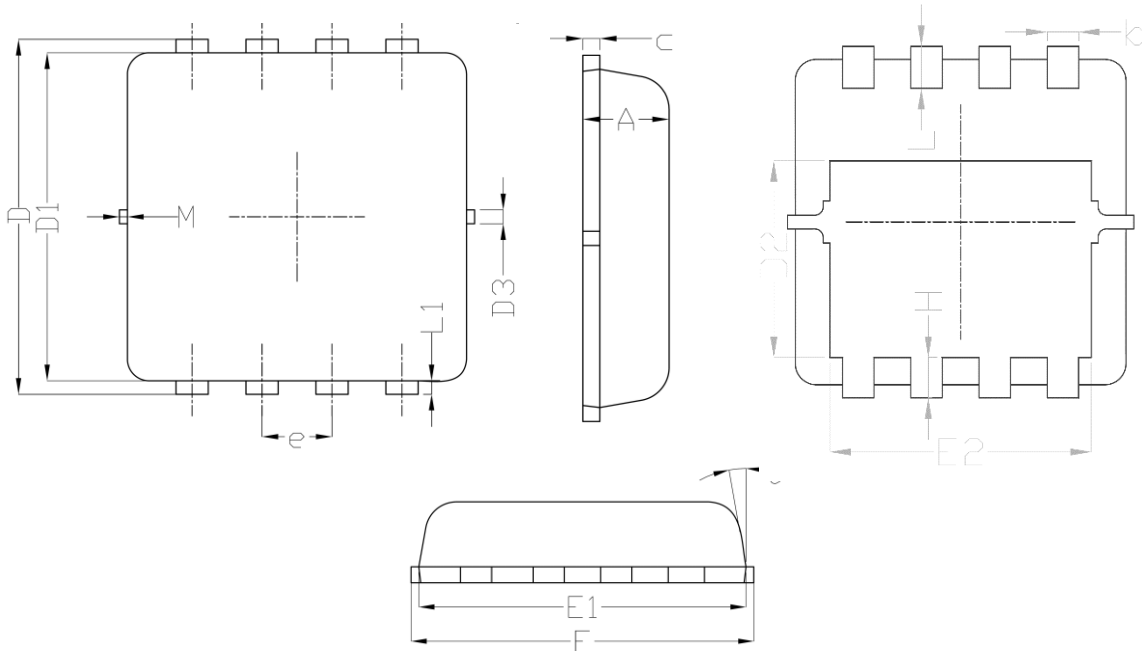


Gate Charge Waveform



Switching Time Waveform

## DFN3.3X3.3A-8 PACKAGE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
b	0.250	0.350	0.010	0.014
c	0.100	0.250	0.004	0.010
D	3.250	3.450	0.128	0.136
D1	3.000	3.200	0.118	0.126
D2	1.780	1.980	0.070	0.078
D3	-	0.130	-	0.005
E	3.200	3.400	0.126	0.134
E1	3.000	3.200	0.118	0.126
E2	2.390	2.590	0.094	0.102
e	0.65BSC.		0.026BSC.	
H	0.300	0.500	0.012	0.020
L	0.300	0.500	0.012	0.020
L1	-	0.130	-	0.005
M	-	0.150	-	0.006
Θ	0°	12°	0°	12°

Recommended Land Pattern

